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Editors:
RAVI K. GULATI
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TESTING OF VLSI CIRCUITS



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Iddq Testing Of Vlsi Circuits

Vijay Nath,Jyotsna Kumar Mandal



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Introduction to IDDQ Testing S. Chakravarty, Paul J. Thadikaran, 2012-12-06 Testing techniques for VLSI circuits are undergoing many exciting changes. The predominant method for testing digital circuits consists of applying a set of input stimuli to the IC and monitoring the logic levels at primary outputs. If for one or more inputs there is a discrepancy between the observed output and the expected output, then the IC is declared to be defective. A new approach to testing digital circuits which has come to be known as IDDQ testing has been actively researched for the last fifteen years. In IDDQ testing, the steady state supply current rather than the logic levels at the primary outputs is monitored. Years of research suggests that IDDQ testing can significantly improve the quality and reliability of fabricated circuits. This has prompted many semiconductor manufacturers to adopt this testing technique among them: Philips Semiconductors, Ford Microelectronics, Intel, Texas Instruments, LSI Logic, Hewlett Packard, SUN microsystems, Alcatel, and SGS Thomson. This increase in the use of IDDQ testing should be of interest to three groups of individuals associated with the IC business: Product Managers and Test Engineers, CAD Tool Vendors, and Circuit Designers. *Introduction to IDDQ Testing* is designed to educate this community. The authors have summarized in one volume the main findings of more than fifteen years of research in this area.

IDDQ Testing of VLSI Circuits Ravi K. Gulati, Charles F. Hawkins, 2012-12-06 Power supply current monitoring to detect CMOS IC defects during production testing quietly laid down its roots in the mid 1970s. Both Sandia Labs and RCA in the United States and Philips Labs in the Netherlands practiced this procedure on their CMOS ICs. At that time, this practice stemmed simply from an intuitive sense that CMOS ICs showing abnormal quiescent power supply current (IDDQ) contained defects. Later, this intuition was supported by data and analysis in the 1980s by Levi RACD Malaiya and Su SUNY Binghamton, Soden and Hawkins, Sandia Labs, and the University of New Mexico, Jacomino and co-workers, Laboratoire d'Automatique de Grenoble, and Maly and co-workers, Carnegie Mellon University. Interest in IDDQ testing has advanced beyond the data reported in the 1980s and is now focused on applications and evaluations involving larger volumes of ICs that improve quality beyond what can be achieved by previous conventional means. In the conventional style of testing, one attempts to propagate the logic states of the suspended nodes to primary outputs. This is done for all or most nodes of the circuit. For sequential circuits, in particular, the complexity of finding suitable tests is very high. In comparison, the IDDQ test does not observe the logic states but measures the integrated current that leaks through all gates. In other words, it is like measuring a patient's temperature to determine the state of health. Despite perceived advantages during the years that followed its initial announcements, skepticism about the practicality of IDDQ testing prevailed. The idea, however, provided a great opportunity to researchers. New results on test generation, fault simulation, design for testability, built-in self-test, and diagnosis for this style of testing have since been reported. After a decade of research, we are definitely closer to practice.

IDDQ testing of VLSI circuits Chuck Hawkins, Keith Baker, 1995

Current Comparator Design for IDDQ Testing in VLSI Circuits Umesh Mehta, 1996

Defect-Oriented Testing for Nano-Metric CMOS VLSI Circuits Manoj Sachdev, José Pineda de Gyvez, 2007-06-04 The 2nd edition of defect oriented testing has been extensively updated New chapters on Functional Parametric Defect Models and Inductive fault Analysis and Yield Engineering have been added to provide a link between defect sources and yield The chapter on RAM testing has been updated with focus on parametric and SRAM stability testing Similarly newer material has been incorporated in digital fault modeling and analog testing chapters The strength of Defect Oriented Testing for nano Metric CMOS VLSIs lies in its industrial relevance

Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits M. Bushnell, Vishwani Agrawal, 2006-04-11 The modern electronic testing has a forty year history Test professionals hold some fairly large conferences and numerous workshops have a journal and there are over one hundred books on testing Still a full course on testing is offered only at a few universities mostly by professors who have a research interest in this area Apparently most professors would not have taken a course on electronic testing when they were students Other than the computer engineering curriculum being too crowded the major reason cited for the absence of a course on electronic testing is the lack of a suitable textbook For VLSI the foundation was provided by semiconductor device technology circuit design and electronic testing In a computer engineering curriculum therefore it is necessary that foundations should be taught before applications The field of VLSI has expanded to systems on a chip which include digital memory and mixed signal subsystems To our knowledge this is the first textbook to cover all three types of electronic circuits We have written this textbook for an undergraduate foundations course on electronic testing Obviously it is too voluminous for a one semester course and a teacher will have to select from the topics We did not restrict such freedom because the selection may depend upon the individual expertise and interests Besides there is merit in having a larger book that will retain its usefulness for the owner even after the completion of the course With equal tenacity we address the needs of three other groups of readers

VLSI Design Dr. M. Nagabushanam, N A *Thermal-Aware Testing of Digital VLSI Circuits and Systems* Santanu Chattopadhyay, 2018-04-24 This book aims to highlight the research activities in the domain of thermal aware testing Thermal aware testing can be employed both at circuit level and at system level Describes range of algorithms for addressing thermal aware test issue presents comparison of temperature reduction with power aware techniques and include results on benchmark circuits and systems for different techniques This book will be suitable for researchers working on power and thermal aware design and the testing of digital VLSI chips

VLSI Testing Stanley Leonard Hurst, 1998 Hurst an editor at the Microelectronics Journal analyzes common problems that electronics engineers and circuit designers encounter while testing integrated circuits and the systems in which they are used and explains a variety of solutions available for overcoming them in both digital and mixed circuits Among his topics are faults in digital circuits generating a digital test pattern signatures and self tests structured design for testability testing structured digital circuits and microprocessors and financial aspects of testing The self contained reference is also suitable as a textbook in a formal course

on the subject Annotation copyrighted by Book News Inc Portland OR *On-Line Testing for VLSI* Michael Nicolaidis, Yervant Zorian, Dhiraj Pradhan, 2013-03-09 Test functions fault detection diagnosis error correction repair etc that are applied concurrently while the system continues its intended function are defined as on line testing In its expanded scope on line testing includes the design of concurrent error checking subsystems that can be themselves self checking fail safe systems that continue to function correctly even after an error occurs reliability monitoring and self test and fault tolerant designs On Line Testing for VLSI contains a selected set of articles that discuss many of the modern aspects of on line testing as faced today The contributions are largely derived from recent IEEE International On Line Testing Workshops Guest editors Michael Nicolaidis Yervant Zorian and Dhiraj Pradhan organized the articles into six chapters In the first chapter the editors introduce a large number of approaches with an expanded bibliography in which some references date back to the sixties On Line Testing for VLSI is an edited volume of original research comprising invited contributions by leading researchers Thermal Testing of Integrated Circuits J. Altet, Antonio Rubio, 2013-03-09 Integrated circuits IC s have undergone a significant evolution in terms of complexity and performance as a result of the substantial advances made in manufacturing technology Circuits in their various mixed formats can be made up tens or even hundreds of millions of devices They work at extremely low voltages and switch at very high frequencies Testing of circuits has become an essential process in IC manufacturing in the effort to ensure that the manufactured components have the appropriate levels of quality Along with the ongoing trend towards more advanced technology and circuit features major testing challenges are continuously emerging The use of ambivalent procedures to test the analogue and digital sections of such complex circuits without interfering in their nominal operation is clearly a critical part of today s technological industries Chapter 1 presents the general purposes and basic concepts related With the testing of integrated circuits discussing the various strategies and their limitations Readers who are already familiar with the field may opt to skip this chapter This book offers a multidisciplinary focus on thermal testing This is a testing method which is not only suitable for use in combination with other existing techniques but is also backed by a wealth of knowledge and offers exciting opportunities in the form of as yet unexplored areas of research and innovation for industrial applications **VLSI and Chip Design** Mr. Rohit Manglik, 2024-07-26 EduGorilla Publication is a trusted name in the education sector committed to empowering learners with high quality study materials and resources Specializing in competitive exams and academic support EduGorilla provides comprehensive and well structured content tailored to meet the needs of students across various streams and levels Proceeding of the Second International Conference on Microelectronics, Computing & Communication Systems (MCCS 2017) Vijay Nath, Jyotsna Kumar Mandal, 2018-07-30 The volume presents high quality papers presented at the Second International Conference on Microelectronics Computing Communication Systems MCCS 2017 The book discusses recent trends in technology and advancement in MEMS and nanoelectronics wireless communications optical communication

instrumentation signal processing image processing bioengineering green energy hybrid vehicles environmental science weather forecasting cloud computing renewable energy RFID CMOS sensors actuators transducers telemetry systems embedded systems and sensor network applications It includes original papers based on original theoretical practical experimental simulations development application measurement and testing The applications and solutions discussed in the book will serve as a good reference material for future works **Istfa '98** ASM International,1998-01-01 **Random**

Testing of Digital Circuits David,2020-11-25 Introduces a theory of random testing in digital circuits for the first time and offers practical guidance for the implementation of random pattern generators signature analyzers design for random testability and testing results Contains several new and unpublished results *VLSI DESIGN* Dr. Udutha

Rajender,Mr.Srikanth Parikibandla,Dr.Arunkumar Madupu ,2022-03-15 VLSI DESIGN BOOK WAS Written BY Dr Udutha Rajender Mr Srikanth Parikibandla Dr Arunkumar Madupu *A Designer's Guide to Built-In Self-Test* Charles E.

Stroud,2005-12-27 A recent technological advance is the art of designing circuits to test themselves referred to as a Built In Self Test This book is written from a designer s perspective and describes the major BIST approaches that have been proposed and implemented along with their advantages and limitations Defect Oriented Testing for CMOS Analog and Digital Circuits

Manoj Sachdev,2013-06-29 Defect oriented testing is expected to play a significant role in coming generations of technology Smaller feature sizes and larger die sizes will make ICs more sensitive to defects that can not be modeled by traditional fault modeling approaches Furthermore with increased level of integration an IC may contain diverse building blocks Such blocks include digital logic PLAs volatile and non volatile memories and analog interfaces For such diverse building blocks traditional fault modeling and test approaches will become increasingly inadequate Defect oriented testing methods have come a long way from a mere interesting academic exercise to a hard industrial reality Many factors have contributed to its industrial acceptance Traditional approaches of testing modern integrated circuits ICs have been found to be inadequate in terms of quality and economics of test In a globally competitive semiconductor market place overall product quality and economics have become very important objectives In addition electronic systems are becoming increasingly complex and demand components of highest possible quality Testing in general and defect oriented testing in particular help in realizing these objectives Defect Oriented Testing for CMOS Analog and Digital Circuits is the first book to provide a complete overview of the subject It is essential reading for all design and test professionals as well as researchers and students working in the field A strength of this book is its breadth Types of designs considered include analog and digital circuits programmable logic arrays and memories Having a fault model does not automatically provide a test Sometimes design for testability hardware is necessary Many design for testability ideas supported by experimental evidence are included from the Foreword by Vishwani D Agrawal **Integrated Circuit Test Engineering** Ian A. Grout,2005-08-22

Using the book and the software provided with it the reader can build his her own tester arrangement to investigate key

aspects of analog digital and mixed system circuits Plan of attack based on traditional testing circuit design and circuit manufacture allows the reader to appreciate a testing regime from the point of view of all the participating interests Worked examples based on theoretical bookwork practical experimentation and simulation exercises teach the reader how to test circuits thoroughly and effectively *On-line Error Detection and Fast Recover Techniques for Dependable Embedded Processors* Matthias Pflanz, 2003-07-31 This book presents a new approach to on line observation and concurrent checking of processors by refining and improving known techniques and introducing new ideas The proposed on line error detection and fast recover techniques support and complement other established methods In combination with other on line observation principles and with a combined hardware software test these techniques are used to fulfill a complete self check scheme for an embedded processor

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