

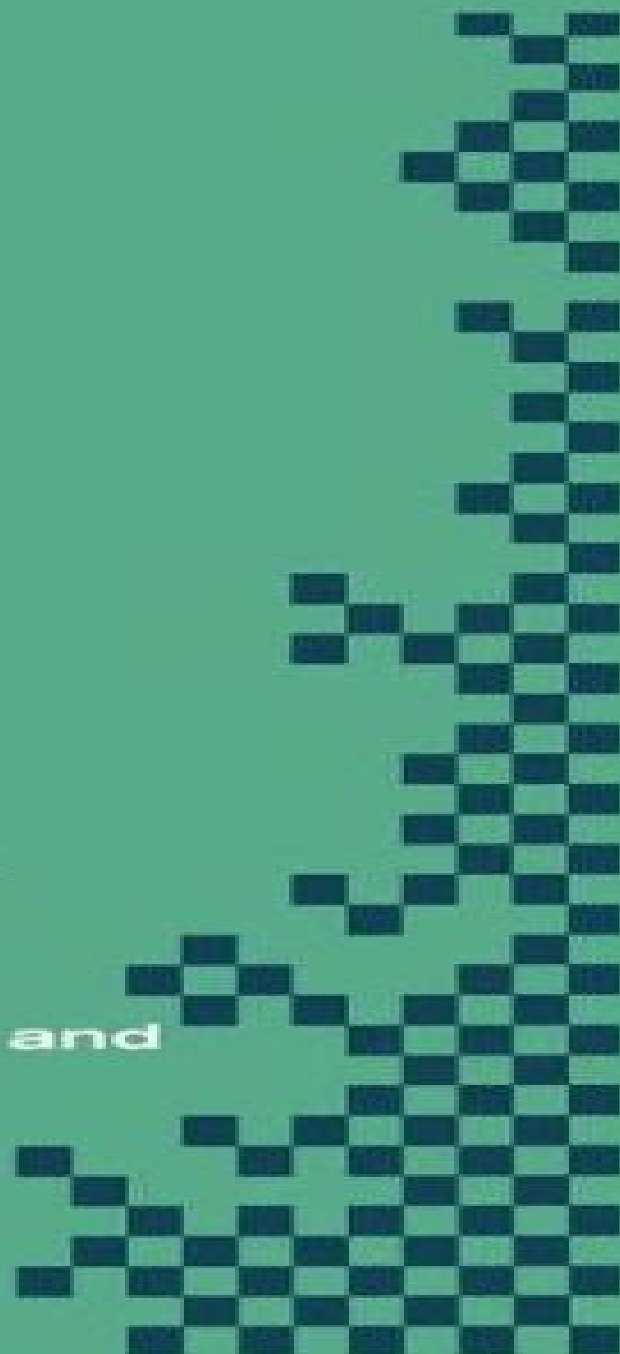
Hardware Description Languages and their Applications

Specification, modelling,
verification and synthesis
of microelectronic systems

Edited by
**Carlos Delgado Kloos and
Eduard Cerny**



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Hardware Description Languages And Their Applications Specification Modelling Verification And Synthesis

Georg Pelz

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Hardware Description Languages And Their Applications Specification Modelling Verification And Synthesis:

Hardware Description Languages and their Applications Carlos Delgado Kloos, Eduard Cerny, 2013-06-05 In the past few decades Computer Hardware Description Languages CHDLs have been a rapidly expanding subject area due to a number of factors including the advancing complexity of digital electronics the increasing prevalence of generic and programmable components of software hardware and the migration of VLSI design to high level synthesis based on HDLs Currently the subject has reached the consolidation phase in which languages and standards are being increasingly used at the same time as the scope is being broadened to additional application areas This book presents the latest developments in this area and provides a forum from which readers can learn from the past and look forward to what the future holds Computer Hardware Description Languages and their Applications D. Borriore, R. Waxman, 2014-06-28 The topic areas presented within this volume focus on design environments and the applications of hardware description and modelling including simulation verification by correctness proofs synthesis and test The strong relationship between the topics of CHDL 91 and the work around the use and re standardization of the VHDL language is also explored The quality of this proceedings and its significance to the academic and professional worlds is assured by the excellent technical programme here compiled

Computer Hardware Description Languages and their Applications D. Agnew, L. Claesen, R. Camposano, 2014-05-21 Hardware description languages HDLs have established themselves as one of the principal means of designing electronic systems The interest in and usage of HDLs continues to spread rapidly driven by the increasing complexity of systems the growth of HDL driven synthesis the research on formal design methods and many other related advances This research oriented publication aims to make a strong contribution to further developments in the field The following topics are explored in depth BDD based system design and analysis system level formal verification formal reasoning on hardware languages for protocol specification VHDL HDL based design methods high level synthesis and text graphical HDLs There are short papers covering advanced design capture and recent work in high level synthesis and formal verification In addition several invited presentations on key issues discuss and summarize recent advances in real time system design automatic verification of sequential circuits and languages for protocol specification *Architecture and Design of Distributed Embedded Systems* Bernd Kleinjohann, 2013-04-18 Due to the decreasing production costs of IT systems applications that had to be realised as expensive PCBs formerly can now be realised as a system on chip Furthermore low cost broadband communication media for wide area communication as well as for the realisation of local distributed systems are available Typically the market requires IT systems that realise a set of specific features for the end user in a given environment so called embedded systems Some examples for such embedded systems are control systems in cars airplanes houses or plants information and communication devices like digital TV mobile phones or autonomous systems like service or edutainment robots For the design of embedded systems the designer has to tackle three major aspects The application itself including the man machine

interface The target architecture of the system including all functional and non functional constraints and the design methodology including modelling specification synthesis test and validation The last two points are a major focus of this book This book documents the high quality approaches and results that were presented at the International Workshop on Distributed and Parallel Embedded Systems DIPES 2000 which was sponsored by the International Federation for Information Processing IFIP and organised by IFIP working groups WG10 3 WG10 4 and WG10 5 The workshop took place on October 18 19 2000 in Schlo Eringerfeld near Paderborn Germany Architecture and Design of Distributed Embedded Systems is organised similar to the workshop Chapters 1 and 4 Methodology I and II deal with different modelling and specification paradigms and the corresponding design methodologies Generic system architectures for different classes of embedded systems are presented in Chapter 2 In Chapter 3 several design environments for the support of specific design methodologies are presented Problems concerning test and validation are discussed in Chapter 5 The last two chapters include distribution and communication aspects Chapter 6 and synthesis techniques for embedded systems Chapter 7 This book is essential reading for computer science researchers and application developers

Advanced VLSI Design and Testability Issues Suman Lata Tripathi, Sobhit Saxena, Sushanta Kumar Mohapatra, 2020-08-19 This book facilitates the VLSI interested individuals with not only in depth knowledge but also the broad aspects of it by explaining its applications in different fields including image processing and biomedical The deep understanding of basic concepts gives you the power to develop a new application aspect which is very well taken care of in this book by using simple language in explaining the concepts In the VLSI world the importance of hardware description languages cannot be ignored as the designing of such dense and complex circuits is not possible without them Both Verilog and VHDL languages are used here for designing The current needs of high performance integrated circuits ICs including low power devices and new emerging materials which can play a very important role in achieving new functionalities are the most interesting part of the book The testing of VLSI circuits becomes more crucial than the designing of the circuits in this nanometer technology era The role of fault simulation algorithms is very well explained and its implementation using Verilog is the key aspect of this book This book is well organized into 20 chapters Chapter 1 emphasizes on uses of FPGA on various image processing and biomedical applications Then the descriptions enlighten the basic understanding of digital design from the perspective of HDL in Chapters 2 5 The performance enhancement with alternate material or geometry for silicon based FET designs is focused in Chapters 6 and 7 Chapters 8 and 9 describe the study of bimolecular interactions with biosensing FETs Chapters 10 13 deal with advanced FET structures available in various shapes materials such as nanowire HFET and their comparison in terms of device performance metrics calculation Chapters 14 18 describe different application specific VLSI design techniques and challenges for analog and digital circuit designs Chapter 19 explains the VLSI testability issues with the description of simulation and its categorization into logic and fault simulation for test pattern generation using Verilog HDL Chapter 20

deals with a secured VLSI design with hardware obfuscation by hiding the IC's structure and function which makes it much more difficult to reverse engineer

NASA Formal Methods Mihaela Bobaru, Klaus Havelund, Gerard Holzmann, Rajeev Joshi, 2011-04-06 This book constitutes the refereed proceedings of the Third International Symposium on NASA Formal Methods NFM 2011 held in Pasadena CA USA in April 2011. The 26 revised full papers presented together with 12 tool papers, 3 invited talks and 2 invited tutorials were carefully reviewed and selected from 141 submissions. The topics covered by NFM 2011 included but were not limited to theorem proving, logic model checking, automated testing and simulation, model based engineering, real time and stochastic systems, SAT and SMT solvers, symbolic execution, abstraction and abstraction refinement, compositional verification techniques, static and dynamic analysis techniques, fault protection, cyber security, specification formalisms, requirements analysis and applications of formal techniques.

Fundamentals and Standards in Hardware Description Languages Jean Mermet, 2012-12-06 The second half of this century will remain as the era of proliferation of electronic computers. They did exist before but they were mechanical. During next century they may perform other mutations to become optical or molecular or even biological. Actually all these aspects are only fancy dresses put on mathematical machines. This was always recognized to be true in the domain of software where machine or high level languages are more or less rigorous but immaterial variations of the universally accepted mathematical language aimed at specifying elementary operations, functions, algorithms and processes. But even a mathematical machine needs a physical support and this is what hardware is all about. The invention of hardware description languages HDLs in the early 60s was an attempt to stay longer at an abstract level in the design process and to push the stage of physical implementation up to the moment when no more technology independent decisions can be taken. It was also an answer to the continuous exponential growth of complexity of systems to be designed. This problem is common to hardware and software and may explain why the syntax of hardware description languages has followed with a reasonable delay of ten years the evolution of the programming languages: at the end of the 60s they were Algol like, a decade later Pascal like and now they are C or ADA like. They have also integrated the new concepts of advanced software specification languages.

Computer Hardware Description Languages and Their Applications John A. Darringer, F. J. Rammig, 1990 Languages for precisely describing the behavior of computers have been studied since the conception of the computer itself. As the computer industry has grown so has the need to exchange information about computers. Computer Hardware Description Languages CHDL are required to provide specifications and detailed implementation for a growing menu of sophisticated design automation tools including synthesis, verification, simulation, analysis, optimization, placement, wiring and testing. Communication requirements and capabilities between suppliers and users of computer components and subsystems facilitate the transfer of new methods and results within the university and industrial research community. As reflected in this book there is an increased emphasis on applications and resulting requirements that are placed on CHDLs. In the field of synthesis a major application area there is

today a focus on high level synthesis and synthesis under design constraints In the area of design correctness research has shifted away from simulation to formal verification techniques such as temporal logic Readings in Hardware/Software Co-Design Giovanni De Micheli,Rolf Ernst,Wayne Wolf,2002 This title serves as an introduction and reference for the field with the papers that have shaped the hardware software co design since its inception in the early 90s *Mechatronic Systems* Georg Pelz,2003-06-02 Covers the modelling and simulation of mechatronic and micromechatronic systems using HDLs Provides an overview of the design of digital and analog circuitry and software for mechatronic systems Presents practical guidance on both chip and systems design for a wide range of mechatronic applications Focuses on a practical approach to the design and simulation of electronic hardware and components of mechatronic systems **Data Converters, Phase-Locked Loops, and Their Applications** Tertulien Ndjountche,2018-09-06 With a focus on designing and verifying CMOS analog integrated circuits the book reviews design techniques for mixed signal building blocks such as Nyquist and oversampling data converters and circuits for signal generation synthesis and recovery The text details all aspects from specifications to the final circuit of the design of digital to analog converters analog to digital converters phase locked loops delay locked loops high speed input output link transceivers and class D amplifiers Special emphasis is put on calibration methods that can be used to compensate circuit errors due to device mismatches and semiconductor process variations Gives an overview of data converters phase and delay locked loop architectures highlighting basic operation and design trade offs Focus on circuit analysis methods useful to meet requirements for a high speed and power efficient operation Outlines design challenges of analog integrated circuits using state of the art CMOS processes Presents design methodologies to optimize circuit performance on both transistor and architectural levels Includes open ended circuit design case studies

High-Level Verification Sudipta Kundu,Sorin Lerner,Rajesh K. Gupta,2011-05-18 Given the growing size and heterogeneity of Systems on Chip SOC the design process from initial specification to chip fabrication has become increasingly complex This growing complexity provides incentive for designers to use high level languages such as C SystemC and SystemVerilog for system level design While a major goal of these high level languages is to enable verification at a higher level of abstraction allowing early exploration of system level designs the focus so far for validation purposes has been on traditional testing techniques such as random testing and scenario based testing This book focuses on high level verification presenting a design methodology that relies upon advances in synthesis techniques as well as on incremental refinement of the design process These refinements can be done manually or through elaboration tools This book discusses verification of specific properties in designs written using high level languages as well as checking that the refined implementations are equivalent to their high level specifications The novelty of each of these techniques is that they use a combination of formal techniques to do scalable verification of system designs completely automatically The verification techniques presented in this book include methods for verifying properties of high level designs and methods for verifying

that the translation from high level design to a low level Register Transfer Language RTL design preserves semantics Used together these techniques guarantee that properties verified in the high level design are preserved through the translation to low level RTL

Models, Methods, and Tools for Complex Chip Design Jan Haase, 2013-09-18 This book brings together a selection of the best papers from the fifteenth edition of the Forum on Specification and Design Languages Conference FDL which was held in September 2012 at Vienna University of Technology Vienna Austria FDL is a well established international forum devoted to dissemination of research results practical experiences and new ideas in the application of specification design and verification languages to the design modeling and verification of integrated circuits complex hardware software embedded systems and mixed technology systems

Formal Methods in Computer-Aided Design Mandayam Srivas, Albert Camilleri, 1996-10-23 This book constitutes the refereed proceedings of the First International Conference on Formal Methods in Computer Aided Design FMCAD 96 held in Palo Alto California USA in November 1996 The 25 revised full papers presented were selected from a total of 65 submissions also included are three invited survey papers and four tutorial contributions The volume covers all relevant formal aspects of work in computer aided systems design including verification synthesis and testing

ESL Models and their Application Brian Bailey, Grant Martin, 2009-12-15 This book arises from experience the authors have gained from years of work as industry practitioners in the field of Electronic System Level design ESL At the heart of all things related to Electronic Design Automation EDA the core issue is one of models what are the models used for what should the models contain and how should they be written and distributed Issues such as interoperability and tool transportability become central factors that may decide which ones are successful and those that cannot get sufficient traction in the industry to survive Through a set of real examples taken from recent industry experience this book will distill the state of the art in terms of System Level Design models and provide practical guidance to readers that can be put into use This book is an invaluable tool that will aid readers in their own designs reduce risk in development projects expand the scope of design projects and improve developmental processes and project planning

Analog and Mixed-Signal Hardware Description Language A. Vachoux, Jean-Michel Bergé, Oz Levia, Jacques Rouillard, 2012-12-06 Hardware description languages HDL such as VHDL and Verilog have found their way into almost every aspect of the design of digital hardware systems Since their inception they gradually proved to be an essential part of modern design methodologies and design automation tools ever exceeding their original goals of being description and simulation languages Their use for automatic synthesis formal proof and testing are good examples So far HDLs have been mainly dealing with digital systems However integrated systems designed today require more and more analog parts such as A D and D A converters phase locked loops current mirrors etc The verification of the complete system therefore asks for the use of a single language Using VHDL or Verilog to handle analog descriptions is possible as it is shown in this book but the real power is coming from true mixed signal HDLs that integrate discrete and continuous semantics into

a unified framework Analog HDLs AHDL are considered here a subset of mixed signal HDLs as they intend to provide the same level of features as HDLs do but with a scope limited to analog systems possibly with limited support of discrete semantics Analog and Mixed Signal Hardware Description Languages covers several aspects related to analog and mixed signal hardware description languages including The use of a digital HDL for the description and the simulation of analog systems The emergence of extensions of existing standard HDLs that provide true analog and mixed signal HDLs The use of analog and mixed signal HDLs for the development of behavioral models of analog electronic building blocks operational amplifier PLL and for the design of microsystems that do not only involve electronic parts The use of a front end tool that eases the description task with the help of a graphical paradigm yet generating AHDL descriptions automatically Analog and Mixed Signal Hardware Description Languages is the first book to show how to use these new hardware description languages in the design of electronic components and systems It is necessary reading for researchers and designers working in electronic design

CONTROL SYSTEMS, ROBOTICS AND AUTOMATION - Volume IV Heinz

Unbehauen,2009-10-11 This Encyclopedia of Control Systems Robotics and Automation is a component of the global Encyclopedia of Life Support Systems EOLSS which is an integrated compendium of twenty one Encyclopedias This 22 volume set contains 240 chapters each of size 5000 30000 words with perspectives applications and extensive illustrations It is the only publication of its kind carrying state of the art knowledge in the fields of Control Systems Robotics and Automation and is aimed by virtue of the several applications at the following five major target audiences University and College Students Educators Professional Practitioners Research Personnel and Policy Analysts Managers and Decision Makers and NGOs

Optimized ASIP Synthesis from Architecture Description Language Models Oliver

Schliebusch,Heinrich Meyr,Rainer Leupers,2007-04-27 New software tools and a sophisticated methodology above RTL are required to answer the challenges of designing an optimized application specific processor ASIP This book offers an automated and fully integrated implementation flow and compares it to common implementation practice Case studies emphasise that neither the architectural advantages nor the design space of ASIPs are sacrificed for an automated implementation Realizing a building block which fulfils the requirements on programmability and computational power is now efficiently possible for the first time Optimized ASIP Synthesis from Architecture Description Language Models inspires hardware designers as well as application engineers to design powerful ASIPs that will make their SoC designs unique

Concise Encyclopedia of Software Engineering Derrick Morris,2013-10-22 This Concise Encyclopedia of Software Engineering is intended to provide compact coverage of the knowledge relevant to the practicing software engineer The content has been chosen to provide an introduction to the theory and techniques relevant to the software of a broad class of computer applications It is supported by examples of particular applications and their enabling technologies This Encyclopedia will be of value to new practitioners who need a concise overview and established practitioners who need to

read about the penumbra surrounding their own specialities It will also be useful to professionals from other disciplines who need to gain some understanding of the various aspects of software engineering which underpin complex information and control systems and the thinking behind them

Model Checking, second edition Edmund M. Clarke, Jr.,Orna Grumberg,Daniel Kroening,Doron Peled,Helmut Veith,2018-12-04 An expanded and updated edition of a comprehensive presentation of the theory and practice of model checking a technology that automates the analysis of complex systems Model checking is a verification technology that provides an algorithmic means of determining whether an abstract model representing for example a hardware or software design satisfies a formal specification expressed as a temporal logic formula If the specification is not satisfied the method identifies a counterexample execution that shows the source of the problem Today many major hardware and software companies use model checking in practice for verification of VLSI circuits communication protocols software device drivers real time embedded systems and security algorithms This book offers a comprehensive presentation of the theory and practice of model checking covering the foundations of the key algorithms in depth The field of model checking has grown dramatically since the publication of the first edition in 1999 and this second edition reflects the advances in the field Reorganized expanded and updated the new edition retains the focus on the foundations of temporal logic model while offering new chapters that cover topics that did not exist in 1999 propositional satisfiability SAT based model checking counterexample guided abstraction refinement and software model checking The book serves as an introduction to the field suitable for classroom use and as an essential guide for researchers

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