

Transactions Briefs

Highly-Parallel Decoding Architectures for Convolutional Turbo Codes

Zhiyong He, Paul Fortier, and Sébastien Roy

Abstract—Highly parallel decoders for convolutional turbo codes have been studied by proposing two parallel decoding architectures and a design approach of parallel interleavers. To solve the memory conflict problem of extrinsic information in a parallel decoder, a block-like approach in which data is written row-by-row and read diagonal-wise is proposed for designing collision-free parallel interleavers. Furthermore, a warm-up-free parallel sliding window architecture is proposed for long turbo codes to maximize the decoding speeds of parallel decoders. The proposed architecture increases decoding speed by 6%–34% at a cost of a storage increase of 1% for an eight-parallel decoder. For short turbo codes (e.g., length of 512 bits), a warm-up-free parallel window architecture is proposed to double the speed at the cost of a hardware increase of 12%.

Index Terms—Decoder, interleaver, parallel architecture, turbo code.

I. INTRODUCTION

Turbo codes [1] have received a lot of interest because of their excellent performance. To apply turbo codes in high-speed digital communications, such as in broadband wireless access based on the IEEE 802.16 standard supporting data rates of up to 70 Mb/s, and in fourth generation cellular systems, which are expected to provide a data rate ranging from 20 to 100 Mb/s for high mobility, high throughput of turbo codes is a critical issue. Since turbo decoders inherently have a large latency and low throughput due to the iterative decoding process, highly parallel decoding architectures are required to achieve speed-up of an order of magnitude.

This paper discusses several key problems in the implementation of highly parallel decoders. One of the most immediate problems is memory conflict during decoding [2], where several component decoders simultaneously get access to the same memory module when reading (writing) the extrinsic information from (into) the memory modules. To avoid collisions in accesses to the memory modules, this paper presents an efficient approach for designing collision-free parallel interleavers in which data is written row-by-row and read diagonal-wise.

The second problem in the implementation of a highly parallel decoder is concerned with limiting both the hardware cost and the decoding delay of the decoder when employing many component decoders. In order to reduce computational complexity, the maximum

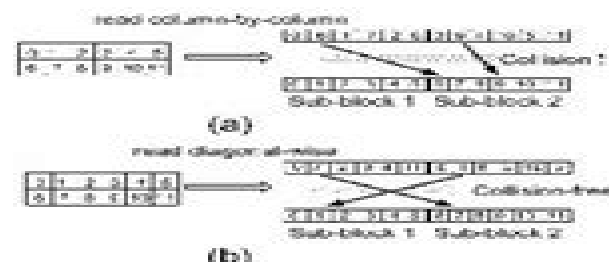


Fig. 1. (a) Interleaver in collision. (b) Collision-free interleaver.

a posteriori probability (MAP) algorithm [3], which is used for decoding convolutional turbo codes is generally implemented in the log-arithmic domain, resulting in the so-called log-MAP algorithm. In an M -parallel decoder based on the log-MAP algorithm, an information block is divided into M sub-blocks which are assigned to M component decoders. To initialize the path metrics in each sub-block, these component decoders typically have to perform a warm-up phase which consumes a few clock cycles at each iteration (e.g., [4]). However, the warm-up phase reduces the throughput substantially when the number of sub-blocks is large.

This paper proposes two warm-up-free parallel architectures for decoding short and long turbo codes. A complete analysis of the two architectures for various code lengths is given based on the 8-state turbo code specified by both the 3GPP standard [5] and the IEEE 802.16 standard.

This paper is organized as follows. Section II describes in detail the approach for designing highly parallel interleavers. Section III proposes warm-up-free sliding window (SW) architectures for highly parallel decoders and then compares BER performance and decoding speeds of the warm-up-free SW architectures with that of the conventional SW architecture. Section IV presents a warm-up-free parallel window architecture for implementing highly parallel decoders with short code lengths. Finally, Section V concludes this paper.

II. PARALLEL INTERLEAVER DESIGN

A. Collisions in a Highly Parallel Decoder

To observe the problem of memory conflict in a parallel decoder, Fig. 1 illustrates an example for an interleaver having a block length of 12 bits. In a two-parallel turbo-decoder, each block is divided into two sub-blocks, each consisting of 6 bits. Let 12 bits be written row-by-row into a 2×6 matrix. Fig. 1(a) shows the designed interleaver when the bits are read column-by-column from the matrix. The solid arrows which show the mapping of the second bits in two sub-blocks, highlight an obvious collision. Indeed, the component decoders have to write the data into the same storage module after decoding the second bits.

Collisions in a highly parallel decoder are further analyzed by using two commonly-used approaches to the design of interleavers for turbo codes, the so-called S -random interleaver (e.g., [6]) and the interleaver specified in the 3GPP standard [5]. Let the input signals

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