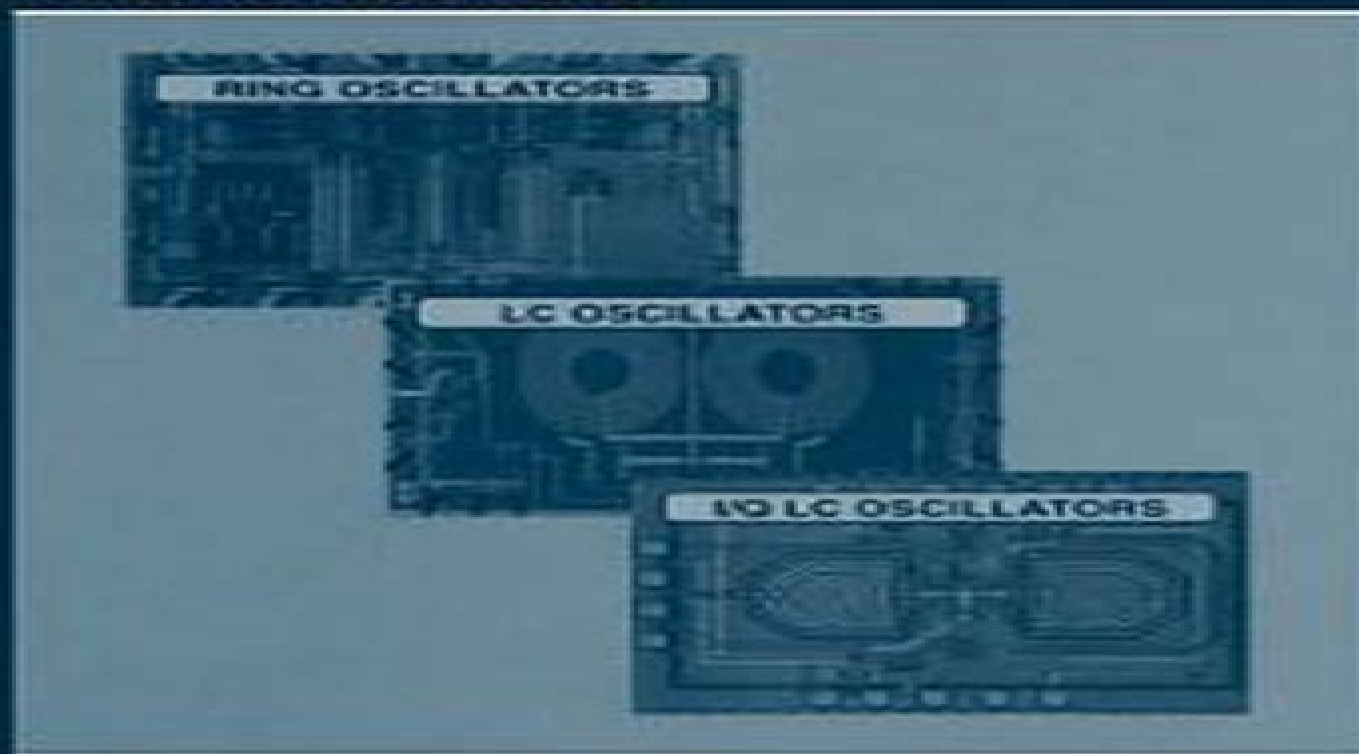


High-Frequency Oscillator Design for Integrated Transceivers

Johan van der Tang, Dieter Kasperkovitz and
Arthur van Roermund



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Highfrequency Oscillator Design For Integrated Transceivers

**J. van der Tang, Dieter
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Highfrequency Oscillator Design For Integrated Transceivers:

High-Frequency Oscillator Design for Integrated Transceivers J. van der Tang, Dieter Kasperkovitz, Arthur H.M. van Roermund, 2006-01-12 This text covers the analysis and design of all high frequency oscillators required to realize integrated transceivers for wireless and wired applications Starting with an in depth review of basic oscillator theory the authors provide a detailed analysis of many oscillator types and circuit topologies

High-Frequency Oscillator Design for Integrated Transceivers J. van der Tang, Dieter Kasperkovitz, Arthur van Roermund, 2008-11-01 This text covers the analysis and design of all high frequency oscillators required to realize integrated transceivers for wireless and wired applications Starting with an in depth review of basic oscillator theory the authors provide a detailed analysis of many oscillator types and circuit topologies

High Frequency Oscillator Design for Integrated Transceivers Johan David van der Tang, Johan van der Tang, 2002

High-speed Optical Transceivers: Integrated Circuits Designs And Optical Devices Techniques Yuyu Liu, Huazhong Yang, 2006-03-09 This book explores the unique advantages and large inherent transmission capacity of optical fiber communication systems The long term and high risk research challenges of optical transceivers are analyzed with a view to sustaining the seemingly insatiable demand for bandwidth A broad coverage of topics relating to the design of high speed optical devices and integrated circuits oriented to low power low cost and small area is discussed Written by specialists with many years of research and engineering experience in the field of optical fiber communication this book is essential for an audience dedicated to the development of integrated electronic systems for optical communication applications It can also be used as a supplementary text for graduate courses on optical transceiver IC design

Design of Very High-Frequency Multirate Switched-Capacitor Circuits Ben U Seng Pan, Rui Paulo da Silva Martins, Jose de Albuquerque Epifanio da Franca, 2006-07-02 Design of Very High Frequency Multirate Switched Capacitor Circuits presents the theory and the corresponding CMOS implementation of the novel multirate sampled data analog interpolation technique which has its great potential on very high frequency analog frond end filtering due to its inherent dual advantage of reducing the speed of data converters and DSP core together with the specification relaxation of the post continuous time filtering This technique completely eliminates the traditional phenomenon of sampled and hold frequency shaping at the lower input sampling rate Also in order to tackle physical IC imperfections at very high frequency the state of the art circuit design and layout techniques for high speed Switched Capacitor SC circuits are comprehensively discussed Optimum circuit architecture tradeoff analysis Simple speed and power trade off analysis of active elements High order filtering response accuracy with respect to capacitor ratio mismatches Time interleaved effect with respect to gain and offset mismatch Time interleaved effect with respect to timing skew and random jitter with non uniformly holding Stage noise analysis and allocation scheme Substrate and supply noise reduction Gain and offset compensation techniques High bandwidth low power amplifier design and layout Very low timing skew multiphase generation Two tailor made optimum design examples in CMOS are presented

The first one achieves a 3 stage 8 fold SC interpolating filter with 5 5MHz bandwidth and 108MHz output sampling rate for a NTSC PAL CCIR 601 digital video at 3 V Another is a 15 tap 57MHz SC FIR bandpass interpolating filter with 4 fold sampling rate increase to 320MHz and the first time embedded frequency band up translation for DDFS system at 2.5V The corresponding chip prototype achieves so far the highest operating frequency highest filter order and highest center frequency with highest dynamic range under the lowest supply voltage when compared to the previously reported high frequency SC filters in CMOS

LNA-ESD Co-Design for Fully Integrated CMOS Wireless Receivers Paul Leroux, Michiel Steyaert, 2006-03-30 LNA ESD Co Design for Fully Integrated CMOS Wireless Receivers fits in the quest for complete CMOS integration of wireless receiver front ends With a combined discussion of both RF and ESD performance it tackles one of the final obstacles on the road to CMOS integration The book is conceived as a design guide for those actively involved in the design of CMOS wireless receivers The book starts with a comprehensive introduction to the performance requirements of low noise amplifiers in wireless receivers Several popular topologies are explained and compared with respect to future technology and frequency scaling The ESD requirements are introduced and related to the state of the art protection devices and circuits LNA ESD Co Design for Fully Integrated CMOS Wireless Receivers provides an extensive theoretical treatment of the performance of CMOS low noise amplifiers in the presence of ESD protection circuitry The influence of the ESD protection parasitics on noise figure gain linearity and matching are investigated Several RF ESD co design solutions are discussed allowing both high RF performance and good ESD immunity for frequencies up to and beyond 5 GHz Special attention is also paid to the layout of both active and passive components LNA ESD Co Design for Fully Integrated CMOS Wireless Receivers offers the reader intuitive insight in the LNA's behavior as well as the necessary mathematical background to optimize its performance All material is experimentally verified with several CMOS implementations among which a fully integrated GPS receiver front end The book is essential reading for RF design engineers and researchers in the field and is also suitable as a text book for an advanced course on the subject

Wireless Technologies Krzysztof Iniewski, 2017-12-19 Advanced concepts for wireless technologies present a vision of technology that is embedded in our surroundings and practically invisible From established radio techniques like GSM 802.11 or Bluetooth to more emerging technologies such as Ultra Wide Band and smart dust motes a common denominator for future progress is the underlying integrated circuit technology Wireless Technologies responds to the explosive growth of standard cellular radios and radically different wireless applications by presenting new architectural and circuit solutions engineers can use to solve modern design problems This reference addresses state of the art CMOS design in the context of emerging wireless applications including 3G 4G cellular telephony wireless sensor networks and wireless medical application Written by top international experts specializing in both the IC industry and academia this carefully edited work uncovers new design opportunities in body area networks medical implants satellite communications automobile radar detection and wearable

electronics The book is divided into three sections wireless system perspectives chip architecture and implementation issues and devices and technologies used to fabricate wireless integrated circuits Contributors address key issues in the development of future silicon based systems such as scale of integration ultra low power dissipation and the integration of heterogeneous circuit design style and processes onto one substrate Wireless sensor network systems are now being applied in critical applications in commerce healthcare and security This reference which contains 25 practical and scientifically rigorous articles provides the knowledge communications engineers need to design innovative methodologies at the circuit and system level

Adaptive Multi-Standard RF Front-Ends Vojkan Vidojkovic, J. van der Tang, Arjan Leeuwenburgh, Arthur H.M. van Roermund, 2008-02-07

N this information era people are living in a society in which processing and exchange of information are vital for their existence Two major issues in such society which are related to processing and exchange of information are connectivity and mobility On one hand computers and Internet provide connectivity and allow communication as well as fast access to large amounts of information On the other hand wireless technologies bring mobility People can move and still be able to communicate and have access to various kind of information Therefore the functioning of an information society is unthinkable without the use of computers Internet and wireless technologies The expectations are that in the future they will merge into a unique system for communication access to information as well as their exchange and processing The era of wireless communications started in 1901 when Guglielmo Marconi successfully transmitted radio signals across the Atlantic Ocean From that moment up to now wireless communications experienced explosive growth and became the fastest growing field in the engineering world Pushed by customer requirements new wireless technologies have been emerging very fast Each new generation of wireless technologies have brought new features and more complexity Pushed by market forces to reduce costs the semiconductor industry has provided new technologies for solid state circuits implementation Fortunately at the same time with the cost reduction performance of new technologies has been improving

60-GHz CMOS Phase-Locked Loops Hammad M. Cheema, Reza Mahmoudi, Arthur H.M. van Roermund, 2010-06-22

Abstract This chapter lays the foundation for the work presented in latter chapters The potential of 60 GHz frequency bands for high data rate wireless transfer is discussed and promising applications are enlisted Furthermore the challenges related to 60 GHz IC design are presented and the chapter concludes with an outline of the book

Keywords Wireless communication 60 GHz Millimeter wave integrated circuit design Phase locked loop CMOS Communication technology has revolutionized our way of living over the last century Since Marconi's transatlantic wireless experiment in 1901 there has been tremendous growth in wireless communication evolving from spark gap telegraphy to today's mobile phones equipped with Internet access and multimedia capabilities The omnipresence of wireless communication can be observed in widespread use of cellular telephony short range communication through wireless local area networks and personal area networks wireless sensors and many others The frequency spectrum from 1 to 6 GHz accommodates the vast majority of current wireless standards and applications

Coupled with the availability of low cost radio frequency RF components and mature integrated circuit IC technologies rapid expansion and implementation of these systems is witnessed The downside of this expansion is the resulting scarcity of available bandwidth and allowable transmit powers In addition stringent limitations on spectrum and energy emissions have been enforced by regulatory bodies to avoid interference between different wireless systems

Mixed-Signal Layout Generation Concepts Chieh Lin, Arthur H.M. van Roermund, Domine Leenaerts, 2005-12-15 This title covers important physical design issues that exist in contemporary analogue and mixed signal design flows The authors bring together many principles and techniques required to successfully develop and implement layout generation tools to accommodate many mixed signal layout generation needs

Static and Dynamic Performance Limitations for High Speed D/A Converters Anne van den Bosch, Michiel Steyaert, Willy M.C. Sansen, 2013-06-29 Static and Dynamic Performance Limitations for High Speed D A Converters discusses the design and implementation of high speed current steering CMOS digital to analog converters Starting from the definition of the basic specifications for a D A converter the elements determining the static and dynamic performance are identified Different guidelines based on scientific derivations are suggested to optimize this performance Furthermore a new closed formula has been derived to account for the influence of the transistor mismatch on the achievable resolution of the current steering D A converter To allow a thorough understanding of the dynamic behavior a new factor has been introduced Moreover the frequency dependency of the output impedance introduces harmonic distortion components which can limit the maximum attainable spurious free dynamic range Finally the last part of the book gives an overview on different existing transistor mismatch models and the link with the static performance of the D A converter

High-Speed Photodiodes in Standard CMOS Technology Sasa Radovanovic, Anne-Johan Annema, Bram Nauta, 2006-10-11 High speed Photodiodes in Standard CMOS Technology describes high speed photodiodes in standard CMOS technology which allow monolithic integration of optical receivers for short haul communication For short haul communication the cost aspect is important and therefore it is desirable that the optical receiver can be integrated in the same CMOS technology as the rest of the system If this is possible then ultimately a single chip system including optical inputs becomes feasible eliminating EMC and crosstalk problems while data rate can be extremely high The problem of photodiodes in standard CMOS technology is that they have very limited bandwidth allowing data rates up to only 50Mbit per second High speed Photodiodes in Standard CMOS Technology first analyzes the photodiode behaviour and compares existing solutions to enhance the speed After this the book introduces a new and robust electronic equalizer technique that makes data rates of 3Gb/s possible without changing the manufacturing technology The application of this technique can be found in short haul fibre communication optical printed circuit boards but also photodiodes for laser disks

Low Power Analog CMOS for Cardiac Pacemakers Fernando Silveira, Denis Flandre, 2013-03-09 Low Power Analog CMOS for Cardiac Pacemakers proposes new techniques for the reduction of power consumption in analog integrated

circuits Our main example is the pacemaker sense channel which is representative of a broader class of biomedical circuits aimed at qualitatively detecting biological signals The first and second chapters are a tutorial presentation on implantable medical devices and pacemakers from the circuit designer point of view This is illustrated by the requirements and solutions applied in our implementation of an industrial IC for pacemakers There from the book discusses the means for reduction of power consumption at three levels base technology power oriented analytical synthesis procedures and circuit architecture

Operational Amplifier Speed and Accuracy Improvement Vadim V. Ivanov,Igor M. Filanovsky,2005-12-30 Operational Amplifier Speed and Accuracy Improvement proposes a new methodology for the design of analog integrated circuits The usefulness of this methodology is demonstrated through the design of an operational amplifier This methodology consists of the following iterative steps description of the circuit functionality at a high level of abstraction using signal flow graphs equivalent transformations and modifications of the graph to the form where all important parameters are controlled by dedicated feedback loops and implementation of the structure using a library of elementary cells Operational Amplifier Speed and Accuracy Improvement shows how to choose structures and design circuits which improve an operational amplifier s important parameters such as speed to power ratio open loop gain common mode voltage rejection ratio and power supply rejection ratio The same approach is used to design clamps and limiting circuits which improve the performance of the amplifier outside of its linear operating region such as slew rate enhancement output short circuit current limitation and input overload recovery

Analog-to-Digital Conversion Marcel J.M. Pelgrom,2010-07-24 A book is like a window that allows you to look into the world The window is shaped by the author and that makes that every window presents a unique view of the world This is certainly true for this book It is shaped by the topics and the projects throughout my career Even more so this book reflects my own style of working and thinking That starts already in Chap 2 When I joined Philips Research in 1979 many of my colleagues used little paper notebooks to keep track of the most used equations and other practical things This notebook was the beginning for Chap 2 a collection of topics that form the basis for much of the other chapters Chapter2 is not intended to explain these topics but to refresh your knowledge and help you when you need some basics to solve more complex issues In the chapters discussing the fundamental processes of conversion you will recognize my preoccupation with mathematics I really enjoy finding an equation that properly describes the underlying mechanism Nevertheless mathematics is not a goal on its own the equations help to understand the way the variables are connected to the result Real insight comes from understanding the physics and electronics In the chapters on circuit design I have tried to reduce the circuit diagrams to the simplest form but not simpler I do have private opinions on what works and what should not be applied

Low-Power Low-Voltage Sigma-Delta Modulators in Nanometer CMOS Libin Yao,Michiel Steyaert,Willy M. C. Sansen,2006-02-06 this book is not suitable for the bookstore catalogue

Systematic Design of Sigma-Delta

Analog-to-Digital Converters Ovidiu Bajdechi,Johan Huijsing,2004-04-30 Systematic Design of Sigma Delta Analog to

Digital Converters describes the issues related to the sigma delta analog to digital converters ADCs design in a systematic manner from the top level of abstraction represented by the filters defining signal and noise transfer functions STF NTF passing through the architecture level where topology related performance is calculated and simulated and finally down to parameters of circuit elements like resistors capacitors and amplifier transconductances used in individual integrators The systematic approach allows the evaluation of different loop filters order aggressiveness discrete time or continuous time implementation with quantizers varying in resolution Topologies explored range from simple single loops to multiple cascaded loops with complex structures including more feedbacks and feedforwards For differential circuits with switched capacitor integrators for discrete time DT loop filters and active RC for continuous time CT ones the passive integrator components are calculated and the power consumption is estimated based on top level requirements like harmonic distortion and noise budget This unified systematic approach to choosing the best sigma delta ADC implementation for a given design target yields an interesting solution for a high resolution broadband DSL like ADC operated at low oversampling ratio which is detailed down to transistor level schematics The target audience of Systematic Design of Sigma Delta Analog to Digital Converters are engineers designing sigma delta ADCs and or switched capacitor and continuous time filters both beginners and experienced It is also intended for students academics involved in sigma delta and analog CAD research

CMOS PLL Synthesizers: Analysis and Design Keliu Shu, Edgar Sanchez-Sinencio, 2006-01-20 Thanks to the advance of semiconductor and communication technology the wireless communication market has been booming in the last two decades It evolved from simple pagers to emerging third generation 3G cellular phones In the meanwhile broadband communication market has also gained a rapid growth As the market always demands hi performance and low cost products circuit designers are seeking hi integration communication devices in cheap CMOS technology The phase locked loop frequency synthesizer is a critical component in communication devices It works as a local oscillator for frequency translation and channel selection in wireless transceivers and broadband cable tuners It also plays an important role as the clock synthesizer for data converters in the analog and digital signal interface This book covers the design and analysis of PLL synthesizers It includes both fundamentals and a review of the state of the art techniques The transient analysis of the third order charge pump PLL reveals its locking behavior accurately The behavioral level simulation of PLL further clarifies its stability limit Design examples are given to clearly illustrate the design procedure of PLL synthesizers A complete derivation of reference spurs in the charge pump PLL is also presented in this book The in depth investigation of the digital CA modulator for fractional N synthesizers provides insightful design guidelines for this important block

Design of Wireless Autonomous Datalogger IC's Wim Claes, Willy M Sansen, Robert Puers, 2006-03-30 Design of Wireless Autonomous Dataloggers IC s reveals the state of the art in the design of complex dataloggers with a special focus on low power consumption The emphasis is on autonomous dataloggers for stand alone applications with remote reprogrammability The book starts with a

comprehensive introduction on the most important design aspects and trade offs for miniaturized low power telemetric dataloggers After the general introduction follows an in depth case study of an autonomous CMOS datalogger IC for the registration of in vivo loads on oral implants After tackling the design of the datalogger on the system level the design of the different building blocks is elaborated in detail with emphasis on low power A clear overview of the operation the implementation and the most important design considerations of the building blocks to achieve optimal system performance is given Design of Wireless Autonomous Dataloggers IC s discusses the design of correlated double sampling amplifiers and sample and holds binary weighted current steering DACs successive approximation ADCs and relaxation clock oscillators and can also be used as a manual for the design of these building blocks Design of Wireless Autonomous Dataloggers IC s covers the complete design flow of low power miniaturized autonomous dataloggers with a bi directional wireless link and on board data processing while providing detailed insight into the most critical design issues of the different building blocks It will allow you to design complex dataloggers faster It is essential reading for analog design engineers and researchers in the field of miniaturized dataloggers and is also suitable as a text for an advanced course on the subject *Systematic Modeling and Analysis of Telecom Frontends and their Building Blocks* Piet Vanassche, Georges Gielen, Willy M Sansen, 2005-10-24 To meet the demands of today s highly competitive market analog electronics designers must develop their IC designs in a minimum of time The difference between first and second time right seriously affects a company s share of the market Analog designers are therefore in need for structured design methods together with the theory and tools to support them especially when pushing the performance limits in high performance designs Systematic Modeling and Analysis of Telecom Frontends and Their Building Blocks aims to help designers in speeding up telecommunication frontend design by offering an in depth understanding of the frontend s behavior together with methods and algorithms that support designers in bringing this understanding to practice The book treats topics such as time varying phase locked loop stability noise in mixing circuits oscillator injection locking oscillator phase noise behavior harmonic oscillator dynamics and many more In doing so it always starts from a theoretical foundation that is both rigorous and general Phase locked loop and mixer analysis for example are grounded upon a general framework for time varying small signal analysis Likewise analysis of harmonic oscillator transient behavior and oscillator phase noise analysis are treated as particular applications of a general framework for oscillator perturbation analysis In order to make the book as easy to read as possible all theory is always accompanied by numerous examples and easy to catch intuitive explanations As such the book is suited for both computer aided design engineers looking for general theories and methods either as background material or for practical implementation in tools as well as for practicing circuit designers looking for help and insight in dealing with a particular application or a particular high performance design problem

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