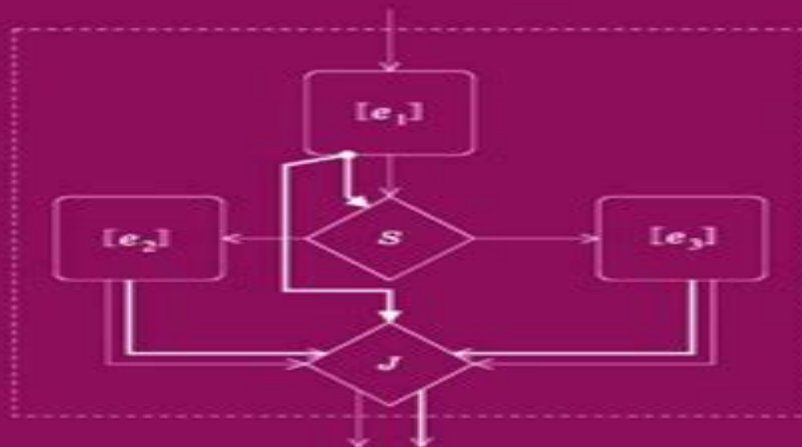


Richard Sharp

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Higher-Level Hardware Synthesis



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Higherlevel Hardware Synthesis

Richard Sharp



Higherlevel Hardware Synthesis:

Higher-Level Hardware Synthesis Richard Sharp,2004-03-12 In the mid 1960s when a single chip contained an average of 50 transistors Gordon Moore observed that integrated circuits were doubling in complexity every year In an influential article published by Electronics Magazine in 1965 Moore predicted that this trend would continue for the next 10 years Despite being criticized for its unrealistic optimism Moore's prediction has remained valid for far longer than even he imagined today chips built using state the art techniques typically contain several million transistors The advances in fabrication technology that have supported Moore's law for four decades have fuelled the computer revolution However this exponential increase in transistor density poses new design challenges to engineers and computer scientists alike New techniques for managing complexity must be developed if circuits are to take full advantage of the vast numbers of transistors available In this monograph we investigate both i the design of high level languages for hardware description and ii techniques involved in translating these high level languages to silicon We propose SAFL a first order functional language designed specifically for behavioral hardware description and describe the implementation of its associated silicon compiler We show that the high level properties of SAFL allow one to exploit program analyses and optimizations that are not employed in existing synthesis systems Furthermore since SAFL fully abstracts the low level details of the implementation technology we show how it can be compiled to a range of different design styles including fully synchronous design and globally asynchronous locally synchronous GALS circuits

Low Power Hardware Synthesis from Concurrent Action-Oriented Specifications Gaurav Singh,Sandeep Kumar Shukla,2010-07-23 Human lives are getting increasingly entangled with technology especially computing and electronics At each step we take especially in a developing world we are dependent on various gadgets such as cell phones handheld PDAs netbooks medical prosthetic devices and medical measurement devices e.g blood pressure monitors glucometers Two important design constraints for such consumer electronics are their form factor and battery life This translates to the requirements of reduction in the die area and reduced power consumption for the semiconductor chips that go inside these gadgets Performance is also important as increasingly sophisticated applications run on these devices and many of them require fast response time The form factor of such electronics goods depends not only on the overall area of the chips inside them but also on the packaging which depends on thermal characteristics Thermal characteristics in turn depend on peak power signature of the chips As a result while the overall energy usage reduction increases battery life peak power reduction influences the form factor One more important aspect of these electronic equipments is that every 6 months or so a newer feature needs to be added to keep ahead of the market competition and hence new designs have to be completed with these new features better form factor battery life and performance every few months This extreme pressure on the time to market is another force that drives the innovations in design automation of semiconductor chips

High-Level VLSI Synthesis Raul Camposano,Wayne Wolf,2012-12-06 The time has come for high

level synthesis When research into synthesizing hardware from abstract program like descriptions started in the early 1970s there was no automated path from the register transfer design produced by high level synthesis to a complete hardware implementation As a result it was very difficult to measure the effectiveness of high level synthesis methods it was also hard to justify to users the need to automate architecture design when low level design had to be completed manually Today's more mature CAD techniques help close the gap between an automatically synthesized design and a manufacturable design Market pressures encourage designers to make use of any and all automated tools Layout synthesis logic synthesis and specialized datapath generators make it feasible to quickly implement a register transfer design in silicon leaving designers more time to consider architectural improvements As IC design becomes more automated customers are increasing their demands today's leading edge designers using logic synthesis systems are training themselves to be tomorrow's consumers of high level synthesis systems The need for very fast turnaround a competitive fabrication market Which makes small quantity ASIC manufacturing possible and the ever growing complexity of the systems being designed all make higher level design automation inevitable

Correct Hardware Design and Verification Methods Tiziana Margaria, Tiziana Margaria-Steffen, Tom F. Melham, 2001-08-27 This book constitutes the refereed proceedings of the 11th IFIP WG 10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods CHARME 2001 held in Livingston Scotland UK in September 2001 The 28 revised full papers and eight short papers presented together with two invited papers and one special paper were carefully reviewed and selected from 56 submissions The book offers topical sections on model checking clocking issues theorem proving with higher order logics hardware compilation tools component verification case studies algorithm verification and duration calculus

Architecting High-Performance Embedded Systems Jim Ledin, 2021-02-05 Explore the complete process of developing systems based on field programmable gate arrays FPGAs including the design of electronic circuits and the construction and debugging of prototype embedded devices Key Features Learn the basics of embedded systems and real time operating systems Understand how FPGAs implement processing algorithms in hardware Design construct and debug custom digital systems from scratch using KiCad Book Description Modern digital devices used in homes cars and wearables contain highly sophisticated computing capabilities composed of embedded systems that generate receive and process digital data streams at rates up to multiple gigabits per second This book will show you how to use Field Programmable Gate Arrays FPGAs and high speed digital circuit design to create your own cutting edge digital systems Architecting High Performance Embedded Systems takes you through the fundamental concepts of embedded systems including real time operation and the Internet of Things IoT and the architecture and capabilities of the latest generation of FPGAs Using powerful free tools for FPGA design and electronic circuit design you will learn how to design build test and debug high performance FPGA based IoT devices The book will also help you get up to speed with embedded system design circuit design hardware construction firmware development and debugging to produce

a high performance embedded device a network based digital oscilloscope You ll explore techniques such as designing four layer printed circuit boards with high speed differential signal pairs and assembling the board using surface mount components By the end of the book you ll have a solid understanding of the concepts underlying embedded systems and FPGAs and will be able to design and construct your own sophisticated digital devices What you will learn Understand the fundamentals of real time embedded systems and sensors Discover the capabilities of FPGAs and how to use FPGA development tools Learn the principles of digital circuit design and PCB layout with KiCad Construct high speed circuit board prototypes at low cost Design and develop high performance algorithms for FPGAs Develop robust reliable and efficient firmware in C Thoroughly test and debug embedded device hardware and firmware Who this book is for This book is for software developers IoT engineers and anyone who wants to understand the process of developing high performance embedded systems You ll also find this book useful if you want to learn about the fundamentals of FPGA development and all aspects of firmware development in C and C Familiarity with the C language digital circuits and electronic soldering is necessary to get started *Field-Programmable Logic: Architectures, Synthesis and Applications* Reiner W.

Hartenstein,1994-08-24 This volume contains the proceedings of the 4th International Workshop on Field Programmable Logic and Applications FPL 94 held in Prague Czech Republic in September 1994 The growing importance of field programmable devices is substantiated by the remarkably high number of 116 submissions for FPL 94 from them the revised versions of 40 full papers and 24 high quality poster presentations were accepted for inclusion in this volume Among the topics treated are testing layout synthesis tools compilation research and CAD trade offs and experience innovations and smart applications FPGA based computer architectures high level design prototyping and ASIC emulators commercial devices new tools CCMs and HW SW co design modelers educational experience and novel architectures **Higher-Level**

Hardware Synthesis Richard Sharp,2004-03-18 In the mid 1960s when a single chip contained an average of 50 transistors Gordon Moore observed that integrated circuits were doubling in complexity every year In an influential article published by Electronics Magazine in 1965 Moore predicted that this trend would continue for the next 10 years Despite being criticized for its unrealistic optimism Moore s prediction has remained valid for far longer than even he imagined today chips built using state the art techniques typically contain several million transistors The advances in fabrication technology that have supported Moore s law for four decades have fuelled the computer revolution However this exponential increase in transistor density poses new design challenges to engineers and computer scientists alike New techniques for managing complexity must be developed if circuits are to take full advantage of the vast numbers of transistors available In this monograph we investigate both i the design of high level languages for hardware description and ii techniques involved in translating these high level languages to silicon We propose SAFL a first order functional language designed specifically for behavioral hardware description and describe the implementation of its associated silicon compiler We show that the high

level properties of SAFL allow one to exploit program analyses and optimizations that are not employed in existing synthesis systems Furthermore since SAFL fully abstracts the low level details of the implementation technology we show how it can be compiled to a range of different design styles including fully synchronous design and globally asynchronous locally synchronous GALS circuits

Research Infrastructures for Hardware Accelerators Yakun Sophia Shao, David Brooks, 2022-05-31 Hardware acceleration in the form of customized datapath and control circuitry tuned to specific applications has gained popularity for its promise to utilize transistors more efficiently Historically the computer architecture community has focused on general purpose processors and extensive research infrastructure has been developed to support research efforts in this domain Envisioning future computing systems with a diverse set of general purpose cores and accelerators computer architects must add accelerator related research infrastructures to their toolboxes to explore future heterogeneous systems This book serves as a primer for the field as an overview of the vast literature on accelerator architectures and their design flows and as a resource guidebook for researchers working in related areas

Hardware Architectures for Post-Quantum Digital Signature Schemes Deepraj Soni, Kanad Basu, Mohammed Nabeel, Najwa Aaraj, Marc Manzano, Ramesh Karri, 2020-10-27 This book explores C based design implementation and analysis of post quantum cryptography PQC algorithms for signature generation and verification The authors investigate NIST round 2 PQC algorithms for signature generation and signature verification from a hardware implementation perspective especially focusing on C based design power performance area security PPAS trade offs and design flows targeting FPGAs and ASICs Describes a comprehensive set of synthesizable C code base as well as the hardware implementations for the different types of PQC algorithms including lattice based code based and multivariate based Demonstrates the hardware FPGA and ASIC and hardware software optimizations and trade offs of the NIST round 2 signature based PQC algorithms Enables designers to build hardware implementations that are resilient to a variety of side channels

Parallel and Distributed Computing, Applications and Technologies Hiroyuki Takizawa, Hong Shen, Toshihiro Hanawa, Jong Hyuk Park, Hui Tian, Ryusuke Egawa, 2023-04-07 This book constitutes the proceedings of the 23rd International Conference on Parallel and Distributed Computing Applications and Technologies PDCAT 2022 which took place in Sendai Japan during December 7-9 2022 The 24 full papers and 16 short papers included in this volume were carefully reviewed and selected from 95 submissions The papers are categorized into the following topical sub headings Heterogeneous System 1 HPC Embedded systems Blockchain Deep Learning Quantum Computing Best Papers Heterogeneous System 2 Equivalence Checking Interconnect Optimization 1 Optimization 2 Privacy and Workflow

Handbook Of Software Engineering And Knowledge Engineering, Vol 2: Emerging Technologies Shi-kuo Chang, 2002-05-10 This is the first handbook to cover comprehensively both software engineering and knowledge engineering two important fields that have become interwoven in recent years Over 60 international experts have contributed to the book Each chapter has been written in such a way that a practitioner of

software engineering and knowledge engineering can easily understand and obtain useful information Each chapter covers one topic and can be read independently of other chapters providing both a general survey of the topic and an in depth exposition of the state of the art Practitioners will find this handbook useful when looking for solutions to practical problems Researchers can use it for quick access to the background current trends and most important references regarding a certain topic The handbook consists of two volumes Volume One covers the basic principles and applications of software engineering and knowledge engineering Volume Two will cover the basic principles and applications of visual and multimedia software engineering knowledge engineering data mining for software knowledge and emerging topics in software engineering and knowledge engineering

System on Chip Design Languages Anne Mignotte,Eugenio Villar,Lynn Horobin,2013-04-17 This book is the third in a series of books collecting the best papers from the three main regional conferences on electronic system design languages HDLCon in the United States APCHDL in Asia Pacific and FDL in Europe Being APCHDL bi annual this book presents a selection of papers from HDLCon Ol and FDL OI HDLCon is the premier HDL event in the United States It originated in 1999 from the merging of the International Verilog Conference and the Spring VHDL User s Forum The scope of the conference expanded from specialized languages such as VHDL and Verilog to general purpose languages such as C and Java In 2001 it was held in February in Santa Clara CA Presentations from design engineers are technical in nature reflecting real life experiences in using HDLs EDA vendors presentations show what is available and what is planned for design tools that utilize HDLs such as simulation and synthesis tools The Forum on Design Languages FDL is the European forum to exchange experiences and learn of new trends in the application of languages and the associated design methods and tools to design complex electronic systems FDL OI was held in Lyon France around seven interrelated workshops Hardware Description Languages Analog and Mixed signal Specification C C HW SW Specification and Design Design Environments Languages Real Time specification for embedded Systems Architecture Modeling and Reuse and System Specification Design Languages

System-Level Design Techniques for Energy-Efficient Embedded Systems Marcus T. Schmitz,Bashir M. Al-Hashimi,Petru Eles,2006-01-16 System Level Design Techniques for Energy Efficient Embedded Systems addresses the development and validation of co synthesis techniques that allow an effective design of embedded systems with low energy dissipation The book provides an overview of a system level co design flow illustrating through examples how system performance is influenced at various steps of the flow including allocation mapping and scheduling The book places special emphasis upon system level co synthesis techniques for architectures that contain voltage scalable processors which can dynamically trade off between computational performance and power consumption Throughout the book the introduced co synthesis techniques which target both single mode systems and emerging multi mode applications are applied to numerous benchmarks and real life examples including a realistic smart phone

Handbook of VLSI Chip Design and Expert Systems A. F. Schwarz,2014-05-10 Handbook of VLSI Chip Design and Expert Systems provides

information pertinent to the fundamental aspects of expert systems which provides a knowledge based approach to problem solving This book discusses the use of expert systems in every possible subtask of VLSI chip design as well as in the interrelations between the subtasks Organized into nine chapters this book begins with an overview of design automation which can be identified as Computer Aided Design of Circuits and Systems CADCAS This text then presents the progress in artificial intelligence with emphasis on expert systems Other chapters consider the impact of design automation which exploits the basic capabilities of computers to perform complex calculations and to handle huge amounts of data with a high speed and accuracy This book discusses as well the characterization of microprocessors The final chapter deals with interactive I O devices This book is a valuable resource for system design experts circuit analysts and designers logic designers device engineers technologists and application specific designers

AI-Enabled Electronic Circuit and System Design Ali Iranmanesh, Hossein Sayadi, 2025-01-27 As our world becomes increasingly digital electronics underpin nearly every industry Understanding how AI enhances this foundational technology can unlock innovations from smarter homes to more powerful gadgets offering vast opportunities for businesses and consumers alike This book demystifies how AI streamlines the creation of electronic systems making them smarter and more efficient With AI s transformative impact on various engineering fields this resource provides an up to date exploration of these advancements authored by experts actively engaged in this dynamic field Stay ahead in the rapidly evolving landscape of AI in engineering with AI Enabled Electronic Circuit and System Design From Ideation to Utilization your essential guide to the future of electronic systems endif A transformative guide describing how revolutionizes electronic design through AI integration Highlighting trends challenges and opportunities Demystifies complex AI applications in electronic design for practical use Leading insights authored by top experts actively engaged in the field Offers a current relevant exploration of significant topics in AI s role in electronic circuit and system design Editor s bios Dr Ali A Iranmanesh is the founder and CEO of Silicon Valley Polytechnic Institute He has received his Bachelor of Science in Electrical Engineering from Sharif University of Technology SUT Tehran Iran and both his master s and Ph D degrees in Electrical Engineering and Physics from Stanford University in Stanford CA He additionally holds a master s degree in business administration MBA from San Jose State University in San Jose CA Dr Iranmanesh is the founder and chairman of the International Society for Quality Electronic Design ISQED Currently he serves as the CEO of Innovotek Dr Iranmanesh has been instrumental in advancing semiconductor technologies innovative design methodologies and engineering education He holds nearly 100 US and international patents reflecting his significant contributions to the field Dr Iranmanesh is the Senior life members of EEE senior member of the American Society for Quality co founder and Chair Emeritus of the IEEE Education Society of Silicon Valley Vice Chair Emeritus of the IEEE PV chapter and recipient of IEEE Outstanding Educator Award Dr Hossein Sayadi is a Tenure Track Assistant Professor and Associate Chair in the Department of Computer Engineering and Computer Science at California State University Long

Beach CSULB He earned his Ph D in Electrical and Computer Engineering from George Mason University in Fairfax Virginia and an M Sc in Computer Engineering from Sharif University of Technology in Tehran Iran As a recognized researcher with over 14 years of research experience Dr Sayadi is the founder and director of the Intelligent Secure and Energy Efficient Computing iSEC Lab at CSULB His research focuses on advancing hardware security and trust AI and machine learning cybersecurity and energy efficient computing addressing critical challenges in modern computing and cyber physical systems He has authored over 75 peer reviewed publications in leading conferences and journals Dr Sayadi is the CSU STEM NET Faculty Fellow with his research supported by multiple National Science Foundation NSF grants and awards from CSULB and the CSU Chancellor s Office He has contributed to various international conferences as an organizer and program committee member including as the TPC Chair for the 2024 and 2025 IEEE ISQED

2nd Workshop on Libraries, Component Modeling and Quality Assurance Eugenio Villar Bonet,1997 Compendio de los trabajos presentados en Toledo durante el 2nd Workshop on Libraries component modeling and quality assurance

Higher Order Logic Theorem Proving and Its Applications Jeffrey J. Joyce,Carl-Johan H. Seger,1994-04-28 This volume constitutes the refereed proceedings of the 1993 Higher Order Logic User s Group Workshop held at the University of British Columbia in August 1993 The workshop was sponsored by the Centre for Integrated Computer System Research It was the sixth in the series of annual international workshops dedicated to the topic of Higher Order Logic theorem proving its usage in the HOL system and its applications The volume contains 40 papers including an invited paper by David Parnas McMaster University Canada entitled Some theorems we should prove

Nanometer CMOS ICs Harry Veendrick,2024-10-21 This textbook provides a comprehensive fully updated introduction to the essentials of nanometer CMOS integrated circuits It includes aspects of scaling to even beyond 3nm CMOS technologies and designs It clearly describes the fundamental CMOS operating principles and presents substantial insight into the various aspects of design fabrication and application Coverage includes all associated disciplines of nanometer CMOS ICs including physics lithography technology design memories VLSI power consumption variability reliability and signal integrity testing yield failure analysis packaging scaling trends and road blocks The text is based upon in house Philips NXP Semiconductors Applied Materials ASML IMEC ST Ericsson Infineon TSMC etc courseware which to date has been completed by more than 7000 engineers working in a large variety of the above mentioned disciplines

SystemC Wolfgang Müller,Wolfgang Rosenstiel,Jürgen Ruf,2007-05-08 SystemC has received a wide acceptance by users and tool vendors as the next generation system description language in order to deal with higher levels of abstraction for complex SoC designs SystemC Methodologies and Applications gives a comprehensive survey on the state of the art of SystemC in industry and research Organised into 11 self contained chapters selected SystemC experts present their approaches in the domains of modelling analysis synthesis Their contributions range from mixed signal and discrete system to embedded software The chapters give a broad overview of recent advances in SystemC methodologies and

applications and are mainly based on presentations given at the European SystemC User Group meetings Logic and Architecture Synthesis Petra Michel, Gabrièle Saucier, 1991 The papers presented in this book cover the whole spectrum from high level synthesis to technology mapping including an overview of fifty years of logic synthesis and asking whether high level synthesis is practical at all The reader will undoubtedly be left with the impression that though the field of synthesis has made considerable progress in the last few years there are still many problems to be dealt with

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