

HIGH-LEVEL POWER ANALYSIS AND OPTIMIZATION

**Anand Raghunathan
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High Level Power Analysis And Optimization

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High Level Power Analysis And Optimization:

High-Level Power Analysis and Optimization Anand Raghunathan, Niraj K. Jha, Sujit Dey, 2012-12-06 High Level Power Analysis and Optimization presents a comprehensive description of power analysis and optimization techniques at the higher architecture and behavior levels of the design hierarchy which are often the levels that yield the most power savings. This book describes power estimation and optimization techniques for use during high level behavioral synthesis as well as for designs expressed at the register transfer or architecture level. High Level Power Analysis and Optimization surveys the state of the art research on the following topics: power estimation, macromodeling techniques for architecture level designs, high level power management techniques and high level synthesis optimizations for low power. High Level Power Analysis and Optimization will be very useful reading for students, researchers, designers, design methodology developers and EDA tool developers who are interested in low power VLSI design or high level design methodologies. High-level Power Analysis and Optimization Techniques Anand Raghunathan, 1997

The VLSI Handbook Wai-Kai Chen, 2018-10-03 For the new millennium Wai Kai Chen introduced a monumental reference for the design analysis and prediction of VLSI circuits. The VLSI Handbook is still a valuable tool for dealing with the most dynamic field in engineering. This second edition includes 13 sections comprising nearly 100 chapters focused on the key concepts, models and equations. Written by a stellar international panel of expert contributors, this handbook is a reliable comprehensive resource for real answers to practical problems. It emphasizes fundamental theory underlying professional applications and also reflects key areas of industrial and research focus. WHAT'S IN THE SECOND EDITION: Sections on Low power electronics and design, VLSI signal processing, Chapters on CMOS fabrication, Content addressable memory, Compound semiconductor, RF circuits, High speed circuit design principles, SiGe HBT technology, Bipolar junction transistor amplifiers, Performance modeling and analysis using SystemC, Design languages expanded from two chapters to twelve, Testing of digital systems. Structured for convenient navigation and loaded with practical solutions, The VLSI Handbook Second Edition remains the first choice for answers to the problems and challenges faced daily in engineering practice.

High Speed CMOS Design Styles Kerry Bernstein, K.M. Carrig, Christopher M. Durham, Patrick R. Hansen, David Hogenmiller, Edward J. Nowak, Norman J. Rohrer, 1998-08-31 High Speed CMOS Design Styles is written for the graduate level student or practicing engineer who is primarily interested in circuit design. It is intended to provide practical reference or horse sense to mechanisms typically described with a more academic slant. This book is organized so that it can be used as a textbook or as a reference book. High Speed CMOS Design Styles provides a survey of design styles in use in industry, specifically in the high speed microprocessor design community. Logic circuit structures, I/O and interface, clocking and timing schemes are reviewed and described. Characteristics, sensitivities and idiosyncrasies of each are highlighted. High Speed CMOS Design Styles also pulls together and explains contributors to performance variability that are associated with process applications conditions and design. Rules of thumb and practical

references are offered Each of the general circuit families is then analyzed for its sensitivity and response to this variability High Speed CMOS Design Styles is an excellent source of ideas and a compilation of observations that highlight how different approaches trade off critical parameters in design and process space

Low-Power High-Level Synthesis for Nanoscale CMOS Circuits Saraju P. Mohanty, Nagarajan Ranganathan, Elias Kougianos, Priyadarsan Patra, 2008-05-31 Low Power High Level Synthesis for Nanoscale CMOS Circuits addresses the need for analysis characterization estimation and optimization of the various forms of power dissipation in the presence of process variations of nano CMOS technologies The authors show very large scale integration VLSI researchers and engineers how to minimize the different types of power consumption of digital circuits The material deals primarily with high level architectural or behavioral energy dissipation because the behavioral level is not as highly abstracted as the system level nor is it as complex as the gate transistor level At the behavioral level there is a balanced degree of freedom to explore power reduction mechanisms the power reduction opportunities are greater and it can cost effectively help in investigating lower power design alternatives prior to actual circuit layout or silicon implementation The book is a self contained low power high level synthesis text for Nanoscale VLSI design engineers and researchers Each chapter has simple relevant examples for a better grasp of the principles presented Several algorithms are given to provide a better understanding of the underlying concepts The initial chapters deal with the basics of high level synthesis power dissipation mechanisms and power estimation In subsequent parts of the text a detailed discussion of methodologies for the reduction of different types of power is presented including Power Reduction Fundamentals Energy or Average Power Reduction Peak Power Reduction Transient Power Reduction Leakage Power Reduction Low Power High Level Synthesis for Nanoscale CMOS Circuits provides a valuable resource for the design of low power CMOS circuits

Low Power Hardware Synthesis from Concurrent Action-Oriented Specifications Gaurav Singh, Sandeep Kumar Shukla, 2010-07-23 Human lives are getting increasingly entangled with technology especially computing and electronics At each step we take especially in a developing world we are dependent on various gadgets such as cell phones handheld PDAs netbooks medical prosthetic devices and medical measurement devices e g blood pressure monitors glucometers Two important design constraints for such consumer electronics are their form factor and battery life This translates to the requirements of reduction in the die area and reduced power consumption for the semiconductor chips that go inside these gadgets Performance is also important as increasingly sophisticated applications run on these devices and many of them require fast response time The form factor of such electronics goods depends not only on the overall area of the chips inside them but also on the packaging which depends on thermal characteristics Thermal characteristics in turn depend on peak power signature of the chips As a result while the overall energy usage reduction increases battery life peak power reduction influences the form factor One more important aspect of these electronic equipments is that every 6 months or so a newer feature needs to be added to keep ahead of the market competition and hence new designs have to be

completed with these new features better form factor battery life and performance every few months This extreme pressure on the time to market is another force that drives the innovations in design automation of semiconductor chips

Low-Power Electronics Design Christian Piguet, 2018-10-03 The power consumption of integrated circuits is one of the most problematic considerations affecting the design of high performance chips and portable devices The study of power saving design methodologies now must also include subjects such as systems on chips embedded software and the future of microelectronics Low Power Electronics Design covers all major aspects of low power design of ICs in deep submicron technologies and addresses emerging topics related to future design This volume explores in individual chapters written by expert authors the many low power techniques born during the past decade It also discusses the many different domains and disciplines that impact power consumption including processors complex circuits software CAD tools and energy sources and management The authors delve into what many specialists predict about the future by presenting techniques that are promising but are not yet reality They investigate nanotechnologies optical circuits ad hoc networks e textiles as well as human powered sources of energy Low Power Electronics Design delivers a complete picture of today s methods for reducing power and also illustrates the advances in chip design that may be commonplace 10 or 15 years from now **Low-Power**

CMOS Circuits Christian Piguet, 2018-10-03 The power consumption of microprocessors is one of the most important challenges of high performance chips and portable devices In chapters drawn from Piguet s recently published Low Power Electronics Design Low Power CMOS Circuits Technology Logic Design and CAD Tools addresses the design of low power circuitry in deep submicron technologies It provides a focused reference for specialists involved in designing low power circuitry from transistors to logic gates The book is organized into three broad sections for convenient access The first examines the history of low power electronics along with a look at emerging and possible future technologies It also considers other technologies such as nanotechnologies and optical chips that may be useful in designing integrated circuits The second part explains the techniques used to reduce power consumption at low levels These include clock gating leakage reduction interconnecting and communication on chips and adiabatic circuits The final section discusses various CAD tools for designing low power circuits This section includes three chapters that demonstrate the tools and low power design issues at three major companies that produce logic synthesizers Providing detailed examinations contributed by leading experts Low Power CMOS Circuits Technology Logic Design and CAD Tools supplies authoritative information on how to design and model for high performance with low power consumption in modern integrated circuits It is a must read for anyone designing modern computers or embedded systems [The Best of ICCAD](#) Andreas Kuehlmann, 2012-12-06 In 2002 the International Conference on Computer Aided Design ICCAD celebrates its 20th anniversary This book commemorates contributions made by ICCAD to the broad field of design automation during that time The foundation of ICCAD in 1982 coincided with the growth of Large Scale Integration The sharply increased functionality of board level circuits led to a major demand for more

powerful Electronic Design Automation EDA tools At the same time LSI grew quickly and advanced circuit integration became widely available This in turn required new tools using sophisticated modeling analysis and optimization algorithms in order to manage the evermore complex design processes Not surprisingly during the same period a number of start up companies began to commercialize EDA solutions complementing various existing in house efforts The overall increased interest in Design Automation DA required a new forum for the emerging community of EDA professionals one which would be focused on the publication of high quality research results and provide a structure for the exchange of ideas on a broad scale Many of the original ICCAD volunteers were also members of CANDE Computer Aided Network Design a workshop of the IEEE Circuits and System Society In fact it was at a CANDE workshop that Bill McCalla suggested the creation of a conference for the EDA professional Bill later developed the name *Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation* Jorge Juan Chico, Enrico Macii, 2003-10-02 Welcome to the proceedings of PATMOS 2003 This was the 13th in a series of international workshops held in several locations in Europe Over the years PATMOS has gained recognition as one of the major European events devoted to power and timing aspects of integrated circuit and system design Despite its significant growth and development PATMOS can still be considered as a very informal forum featuring high level scientific presentations together with open discussions and panel sessions in a free and relaxed environment This year PATMOS took place in Turin Italy organized by the Politecnico di Torino with technical co sponsorship from the IEEE Circuits and Systems Society and the generous support of the European Commission as well as that of several industrial sponsors including BullDAST Cadence Mentor Graphics STMicroelectronics and Synopsys The objective of the PATMOS workshop is to provide a forum to discuss and investigate the emerging problems in methodologies and tools for the design of new generations of integrated circuits and systems A major emphasis of the technical program is on speed and low power aspects with particular regard to modeling characterization design and architectures *Embedded Software for SoC* Ahmed Amine Jerraya, Sungjoo Yoo, Norbert Wehn, Diederik Verkest, 2005-12-30 This title covers all software related aspects of SoC design from embedded and application domain specific operating systems to system architecture for future SoC It will give embedded software designers invaluable insights into the constraints imposed by the use of embedded software in an SoC context *Design of Cost-Efficient Interconnect Processing Units* Marcello Coppola, Miltos D. Grammatikakis, Riccardo Locatelli, Giuseppe Maruccia, Lorenzo Pieralisi, 2020-10-14 Streamlined Design Solutions Specifically for NoC To solve critical network on chip NoC architecture and design problems related to structure performance and modularity engineers generally rely on guidance from the abundance of literature about better understood system level interconnection networks However on chip networks present several distinct challenges that require novel and specialized solutions not found in the tried and true system level techniques A Balanced Analysis of NoC Architecture As the first detailed description of the commercial Spidergon STNoC architecture Design of Cost Efficient Interconnect Processing Units Spidergon STNoC examines the highly

regarded cost cutting technology that is set to replace well known shared bus architectures such as STBus for demanding multiprocessor system on chip SoC applications Employing a balanced well organized structure simple teaching methods numerous illustrations and easy to understand examples the authors explain how the SoC and NoC technology works why developers designed it the way they did the system level design methodology and tools used to configure the Spidergon STNoC architecture differences in cost structure between NoCs and system level networks From professionals in computer sciences electrical engineering and other related fields to semiconductor vendors and investors all readers will appreciate the encyclopedic treatment of background NoC information ranging from CMPs to the basics of interconnection networks The text introduces innovative system level design methodology and tools for efficient design space exploration and topology selection It also provides a wealth of key theoretical and practical MPSoC and NoC topics such as technological deep sub micron effects homogeneous and heterogeneous processor architectures multicore SoC interconnect processing units generic NoC components and embeddings of common communication patterns

Springer Handbook of Automation Shimon Y. Nof, 2009-07-16 Automation is undergoing a major transformation in scope and dimension and plays an increasingly important role in the global economy and in our daily lives Engineers combine automated devices with mathematical and organizational tools to create complex systems for a rapidly expanding range of applications and human activities This handbook incorporates these new developments and presents a widespread and well structured conglomeration of new emerging application areas of automation Besides manufacturing as a primary application of automation the handbook contains new application areas such as medical systems and health transportation security and maintenance service construction and retail as well as production or logistics This Springer Handbook is not only an ideal resource for automation experts but also for people new to this expanding field such as engineers medical doctors computer scientists designers It is edited by an internationally renowned and experienced expert

Multiprocessor System-on-Chip Michael Hübner, Jürgen Becker, 2010-11-25 The purpose of this book is to evaluate strategies for future system design in multiprocessor system on chip MPSoC architectures Both hardware design and integration of new development tools will be discussed Novel trends in MPSoC design combined with reconfigurable architectures are a main topic of concern The main emphasis is on architectures design flow tool development applications and system design

High Level Techniques for Power Estimation, Analysis and Optimization Vamsi Krishna, 1999

Power Aware Design Methodologies Massoud Pedram, Jan M. Rabaey, 2007-05-08 Power Aware Design Methodologies was conceived as an effort to bring all aspects of power aware design methodologies together in a single document It covers several layers of the design hierarchy from technology circuit logic and architectural levels up to the system layer It includes discussion of techniques and methodologies for improving the power efficiency of CMOS circuits digital and analog systems on chip microelectronic systems wirelessly networked systems of computational nodes and so on In addition to providing an in depth analysis of the

sources of power dissipation in VLSI circuits and systems and the technology and design trends this book provides a myriad of state of the art approaches to power optimization and control The different chapters of Power Aware Design Methodologies have been written by leading researchers and experts in their respective areas Contributions are from both academia and industry The contributors have reported the various technologies methodologies and techniques in such a way that they are understandable and useful

Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Vassilis Paliouras, 2005-09-06 This book constitutes the refereed proceedings of the 15th International Workshop on Power and Timing Optimization and Simulation PATMOS 2005 held in Leuven Belgium in September 2005 The 74 revised full papers presented were carefully reviewed and selected from numerous submissions The papers are organized in topical sections on low power processors code optimization for low power high level design telecommunications and signal processing low power circuits system on chip design busses and interconnections modeling design automation low power techniques memory and register files applications digital circuits and analog and physical design

Energy Efficient High Performance Processors Jawad Haj-Yahya, Avi Mendelson, Yosi Ben Asher, Anupam Chattopadhyay, 2018-03-22 This book explores energy efficiency techniques for high performance computing HPC systems using power management methods Adopting a step by step approach it describes power management flows algorithms and mechanism that are employed in modern processors such as Intel Sandy Bridge Haswell Skylake and other architectures e g ARM Further it includes practical examples and recent studies demonstrating how modem processors dynamically manage wide power ranges from a few milliwatts in the lowest idle power state to tens of watts in turbo state Moreover the book explains how thermal and power deliveries are managed in the context this huge power range The book also discusses the different metrics for energy efficiency presents several methods and applications of the power and energy estimation and shows how by using innovative power estimation methods and new algorithms modern processors are able to optimize metrics such as power energy and performance Different power estimation tools are presented including tools that break down the power consumption of modern processors at sub processor core thread granularity The book also investigates software firmware and hardware coordination methods of reducing power consumption for example a compiler assisted power management method to overcome power excursions Lastly it examines firmware algorithms for dynamic cache resizing and dynamic voltage and frequency scaling DVFS for memory sub systems

Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Johan Vounckx, Nadine Azemard, Philippe Maurine, 2006-09-07 This book constitutes the refereed proceedings of the 16th International Workshop on Power and Timing Modeling Optimization and Simulation PATMOS 2006 The book presents 41 revised full papers and 23 revised poster papers together with 4 key notes and 3 industrial abstracts Topical sections include high level design power estimation and modeling memory and register files low power digital circuits busses and interconnects low power techniques applications and SoC design modeling and

more **Electronic Design Automation for IC System Design, Verification, and Testing** Luciano Lavagno, Igor L. Markov, Grant Martin, Louis K. Scheffer, 2017-12-19 The first of two volumes in the Electronic Design Automation for Integrated Circuits Handbook Second Edition Electronic Design Automation for IC System Design Verification and Testing thoroughly examines system level design microarchitectural design logic verification and testing Chapters contributed by leading experts authoritatively discuss processor modeling and design tools using performance metrics to select microprocessor cores for integrated circuit IC designs design and verification languages digital simulation hardware acceleration and emulation and much more New to This Edition Major updates appearing in the initial phases of the design flow where the level of abstraction keeps rising to support more functionality with lower non recurring engineering NRE costs Significant revisions reflected in the final phases of the design flow where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting edge applications and approaches realized in the decade since publication of the previous edition these are illustrated by new chapters on high level synthesis system on chip SoC block based design and back annotating system level models Offering improved depth and modernity Electronic Design Automation for IC System Design Verification and Testing provides a valuable state of the art reference for electronic design automation EDA students researchers and professionals

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