

**SEVENTH IEEE INTERNATIONAL
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High Level Design Validation And Test Workshop Hldvt 2001 Proceedings Of The 6th Ieee International Conference

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High-Level Design, Validation and Test Workshop (HLDVT 2001): Proceedings of the 6th IEEE International Conference
IEEE Computer Society Staff,2001 *Sixth IEEE International High-Level Design Validation and Test Workshop ,2001*
Eighteen full papers and eight short presentations from international engineers and researchers discuss current developments new methodologies and emerging trends in design verification and test The focus of the sixth conference was on hardware software embedded systems and system on chips Topics include for example the automatic validation of pipeline specifications the use of sequential ATPG for model checking formal verification of the Pentium 4 multiplier and using cutwidth to improve symbolic simulation and Boolean satisfiability The volume is not indexed c Book News Inc

Integrated Formal Methods Eerke Boiten,John Derrick,Graeme Smith,2004-03-24 This book constitutes the refereed proceedings of the 4th International Conference on Integrated Formal Methods IFM 2004 held in Canterbury UK in April 2004 The 24 revised full papers presented together with 3 invited papers and one invited tutorial chapter were carefully reviewed and selected from 65 submissions The papers are devoted to automating program analysis state event based verification formalizing graphical notions refinement object orientation hybrid and timed automata integration frameworks verifying interactive systems and testing and assertions **Multiprocessor Systems-on-Chips** Ahmed Jerraya,Wayne Wolf,2005 Modern system on chip SoC design shows a clear trend toward integration of multiple processor cores on a single chip Designing a multiprocessor system on chip MPSOC requires an understanding of the various design styles and techniques used in the multiprocessor Understanding the application area of the MPSOC is also critical to making proper tradeoffs and design decisions Multiprocessor Systems on Chips covers both design techniques and applications for MPSOCs Design topics include multiprocessor architectures processors operating systems compilers methodologies and synthesis algorithms and application areas covered include telecommunications and multimedia The majority of the chapters were collected from presentations made at the International Workshop on Application Specific Multi Processor SoC held over the past two years The workshop assembled internationally recognized speakers on the range of topics relevant to MPSOCs After having refined their material at the workshop the speakers are now writing chapters and the editors are fashioning them into a unified book by making connections between chapters and developing common terminology Examines several different architectures and the constraints imposed on them Discusses scheduling real time operating systems and compilers Analyzes design trade off and decisions in telecommunications and multimedia applications **Educational Recommender Systems and Technologies: Practices and Challenges** Santos, Olga C.,2011-12-31 Recommender systems have shown to be successful in many domains where information overload exists This success has motivated research on how to deploy recommender systems in educational scenarios to facilitate access to a wide spectrum of information Tackling open issues in

their deployment is gaining importance as lifelong learning becomes a necessity of the current knowledge based society Although Educational Recommender Systems ERS share the same key objectives as recommenders for e commerce applications there are some particularities that should be considered before directly applying existing solutions from those applications Educational Recommender Systems and Technologies Practices and Challenges aims to provide a comprehensive review of state of the art practices for ERS as well as the challenges to achieve their actual deployment Discussing such topics as the state of the art of ERS methodologies to develop ERS and architectures to support the recommendation process this book covers researchers interested in recommendation strategies for educational scenarios and in evaluating the impact of recommendations in learning as well as academics and practitioners in the area of technology enhanced learning

Hybrid Optimization Pascal van Hentenryck, Michela Milano, 2010-11-05 Hybrid Optimization focuses on the application of artificial intelligence and operations research techniques to constraint programming for solving combinatorial optimization problems This book covers the most relevant topics investigated in the last ten years by leading experts in the field and speculates about future directions for research This book includes contributions by experts from different but related areas of research including constraint programming decision theory operations research SAT artificial intelligence as well as others These diverse perspectives are actively combined and contrasted in order to evaluate their relative advantages This volume presents techniques for hybrid modeling integrated solving strategies including global constraints decomposition techniques use of relaxations and search strategies including tree search local search and metaheuristics Various applications of the techniques presented as well as supplementary computational tools are also discussed *Index of Conference Proceedings* British Library. Document Supply Centre, 2002

Concurrency and Hardware Design Jordi Cortadella, 2002-11-26 This LNCS State of the Art Survey is devoted to the relatively old and well known behavioral paradigm in computing concurrency and to the ways in which concurrency is exhibited or can be exploited in digital hardware devices The nine chapters presented are organized in four parts on formal methods asynchronous circuits embedded systems design and timed verification and performance analysis

Computer Aided Verification Swarat Chaudhuri, Azadeh Farzan, 2016-07-12 The two volume set LNCS 9779 and LNCS 9780 constitutes the refereed proceedings of the 28th International Conference on Computer Aided Verification CAV 2016 held in Toronto ON USA in July 2016 The total of 46 full and 12 short papers presented in the proceedings was carefully reviewed and selected from 195 submissions The papers were organized in topical sections named probabilistic systems synthesis constraint solving model checking program analysis timed and hybrid systems verification in practice concurrency and automata and games

Fixed-Parameter Linear-Time Algorithms for NP-hard Graph and Hypergraph Problems Arising in Industrial Applications Bevern, René van, 2014-10-01 This thesis aims for the development of efficient algorithms to exactly solve four selected NP hard graph and hypergraph problems arising in the fields of scheduling steel manufacturing software

engineering radio frequency allocation computer aided circuit design and social network analysis NP hard problems presumably cannot be solved exactly in a running time growing only polynomially with the input size In order to still solve the considered problems efficiently this thesis develops linear time data reduction and fixed parameter linear time algorithms that can be proven to run in linear time if certain parameters of the problem instances are constant Besides proving linear worst case running times the efficiency of most of the developed algorithms is evaluated experimentally Moreover the limits of fixed parameter linear time algorithms and provably efficient and effective data reduction are shown Diese Dissertation besch ftigt sich mit der Entwicklung effizienter Algorithmen zur exakten L sung vier ausgew hltter NP schwerer Probleme aus der Ablaufplanung Stahlverarbeitung Softwaretechnik Frequenzzuteilung aus der computergest tzten Hardwareentwicklung und der Analyse sozialer Netzwerke NP schwere Probleme k nnen vermutlich nicht optimal in einer polynomiell mit der Eingabegr e wachsenden Zeit gel st werden Um sie dennoch effizient zu l sen entwickelt diese Arbeit Linearzeitdatenreduktionsalgorithmen und Festparameter Linearzeitalgorithmen Algorithmen die beweisbar in Linearzeit laufen wenn bestimmte Parameter der Probleminstanzen konstant sind Hierbei wird nicht nur bewiesen dass die entwickelten Algorithmen in Linearzeit laufen es findet zus tzlich eine experimentelle Evaluation der meisten der entwickelten Algorithmen statt Ferner werden die Grenzen von Festparameter Linearzeitalgorithmen und beweisbar effizienter und effektiver Datenreduktion aufgezeigt

Automated Reasoning with Analytic Tableaux and Related Methods Marta Cialdea Mayer, Fiora Pirri, 2003-10-24 This book constitutes the refereed proceedings of the International Conference on Automated Reasoning with Analytic Tableaux and Related Methods TABLEUX 2003 held in Rome Italy in September 2003 The 20 revised full papers presented were carefully reviewed and selected for inclusion in the book All current issues surrounding the mechanization of logical reasoning with tableaux and similar methods are addressed in the context of a broad variety of logic calculi

Handbook of Computer Architecture Anupam Chattopadhyay, 2024-12-20 This handbook presents the key topics in the area of computer architecture covering from the basic to the most advanced topics including software and hardware design methodologies It will provide readers with the most comprehensive updated reference information covering applications in single core processors multicore processors application specific processors reconfigurable architectures emerging computing architectures processor design and programming flows test and verification This information benefits the readers as a full and quick technical reference with a high level review of computer architecture technology detailed technical descriptions and the latest practical applications

Energy-Efficient Wireless Sensor Networks Vidushi Sharma, Anuradha Pughat, 2017-07-28 The advances in low power electronic devices integrated with wireless communication capabilities are one of recent areas of research in the field of Wireless Sensor Networks WSNs One of the major challenges in WSNs is uniform and least energy dissipation while increasing the lifetime of the network This is the first book that introduces the energy efficient wireless sensor network techniques and protocols The text covers the

theoretical as well as the practical requirements to conduct and trigger new experiments and project ideas The advanced techniques will help in industrial problem solving for energy hungry wireless sensor network applications Correct Hardware Design and Verification Methods Dominique Borrione,Wolfgang Paul,2005-10-07 This book constitutes the refereed proceedings of the 13th IFIP WG 10 5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods CHARME 2005 held in Saarbrücken Germany in October 2005 The 21 revised full papers and 18 short papers presented together with 2 invited talks and one tutorial were carefully reviewed and selected from 79 submissions The papers are organized in topical sections on functional approaches to design description game solving approaches abstraction algorithms and techniques for speeding DD based verification real time and LTL model checking evaluation of SAT based tools model reduction and verification of memory hierarchy mechanisms **Computer Aided Verification** Warren A. Hunt, Jr.,Fabio Somenzi,2011-05-02 The refereed proceedings of the 15th International Conference on Computer Aided Verification CAV 2003 held in Boulder CO USA in July 2003 The 32 revised full papers and 9 tool papers presented were carefully reviewed and selected from a total of 102 submissions The papers are organized in topical sections on bounded model checking symbolic model checking games trees and counters tools abstraction dense time infinite state systems applications theorem proving automata based verification invariants and explicit model checking **Post-Silicon and Runtime Verification for Modern Processors** Ilya Wagner,Valeria Bertacco,2010-11-25 The purpose of this book is to survey the state of the art and evolving directions in post silicon and runtime verification The authors start by giving an overview of the state of the art in verification particularly current post silicon methodologies in use in the industry both for the domain of processor pipeline design and for memory subsystems They then dive into the presentation of several new post silicon verification solutions aimed at boosting the verification coverage of modern processors dedicating several chapters to this topic The presentation of runtime verification solutions follows a similar approach This is an area of processor design that is still in its early stages of exploration and that holds the promise of accomplishing the ultimate goal of achieving complete correctness guarantees for microprocessor based computation The authors conclude the book with a look towards the future of late stage verification and its growing role in the processor life cycle Books in Print Supplement ,2002

Optimizing Mapping in System Level Design Qi Zhu,2008 **IBM Systems Journal** International Business Machines Corporation,2002 Special Issue on Design Validation of Large Systems (from Proceedings of IEEE HLDVT 2004) Ian G. Harris,2003

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