

# High Level Synthesis of Pipelined Datapaths

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# High Level Synthesis Of Pipelined Datapaths

**Justin Davis, Robert Reese**



## High Level Synthesis Of Pipelined Datapaths:

**High Level Synthesis of Pipelined Datapaths** Péter Arató,Tamás Visegrády,István Jankovits,2001-03-16 CD ROM features a step by step PIPE tutorial     High-level Synthesis of Pipelined Datapaths Arató Péter,2000     Low-Power High-Level Synthesis for Nanoscale CMOS Circuits Saraju P. Mohanty,Nagarajan Ranganathan,Elias Kougianos,Priyardarsan Patra,2008-05-31 Low Power High Level Synthesis for Nanoscale CMOS Circuits addresses the need for analysis characterization estimation and optimization of the various forms of power dissipation in the presence of process variations of nano CMOS technologies The authors show very large scale integration VLSI researchers and engineers how to minimize the different types of power consumption of digital circuits The material deals primarily with high level architectural or behavioral energy dissipation because the behavioral level is not as highly abstracted as the system level nor is it as complex as the gate transistor level At the behavioral level there is a balanced degree of freedom to explore power reduction mechanisms the power reduction opportunities are greater and it can cost effectively help in investigating lower power design alternatives prior to actual circuit layout or silicon implementation The book is a self contained low power high level synthesis text for Nanoscale VLSI design engineers and researchers Each chapter has simple relevant examples for a better grasp of the principles presented Several algorithms are given to provide a better understanding of the underlying concepts The initial chapters deal with the basics of high level synthesis power dissipation mechanisms and power estimation In subsequent parts of the text a detailed discussion of methodologies for the reduction of different types of power is presented including Power Reduction Fundamentals Energy or Average Power Reduction Peak Power Reduction Transient Power Reduction Leakage Power Reduction Low Power High Level Synthesis for Nanoscale CMOS Circuits provides a valuable resource for the design of low power CMOS circuits     **Accelerator Data-Path Synthesis for High-Throughput Signal Processing Applications** Werner Geurts,Francky Catthoor,Serge Vernalde,Hugo De Man,2011-06-27 Accelerator Data Path Synthesis for High Throughput Signal Processing Applications is the first book to show how to use high level synthesis techniques to cope with the stringent timing requirements of complex high throughput real time signal and data processing The book describes the state of the art in architectural synthesis for complex high throughput real time processing Unlike many other the Synthesis approach used in this book targets an architecture style or an application domain This approach is thus heavily application driven and this is illustrated in the book by several realistic demonstration examples used throughout Accelerator Data Path Synthesis for High Throughput Signal Processing Applications focuses on domains where application specific high speed solutions are attractive such as significant parts of audio telecom instrumentation speech robotics medical and automotive processing image and video processing TV multi media radar sonar etc Moreover it addresses mainly the steps above the traditional scheduling and allocation tasks which focus on scalar operations and data Accelerator Data Path Synthesis for High Throughput Signal Processing Applications is of interest to researchers senior design engineers and

CAD managers both in academia and industry It provides an excellent overview of what capabilities to expect from future practical design tools and includes an extensive bibliography

**Domain Specific High-Level Synthesis for Cryptographic Workloads** Ayesha Khalid,Goutam Paul,Anupam Chattopadhyay,2019-03-28 This book offers an in depth study of the design and challenges addressed by a high level synthesis tool targeting a specific class of cryptographic kernels i e symmetric key cryptography With the aid of detailed case studies it also discusses optimization strategies that cannot be automatically undertaken by CRYKET Cryptographic kernels toolkit The dynamic nature of cryptography where newer cryptographic functions and attacks frequently surface means that such a tool can help cryptographers expedite the very large scale integration VLSI design cycle by rapidly exploring various design alternatives before reaching an optimal design option Features include flexibility in cryptographic processors to support emerging cryptanalytic schemes area efficient multinational designs supporting various cryptographic functions and design scalability on modern graphics processing units GPUs These case studies serve as a guide to cryptographers exploring the design of efficient cryptographic implementations

High — Level Synthesis Daniel D. Gajski,Nikil D. Dutt,Allen C-H Wu,Steve Y-L Lin,2012-12-06 Research on high level synthesis started over twenty years ago but lower level tools were not available to seriously support the insertion of high level synthesis into the mainstream design methodology Since then substantial progress has been made in formulating and understanding the basic concepts in high level synthesis Although many open problems remain high level synthesis has matured High Level Synthesis Introduction to Chip and System Design presents a summary of the basic concepts and results and defines the remaining open problems This is the first textbook on high level synthesis and includes the basic concepts the main algorithms used in high level synthesis and a discussion of the requirements and essential issues for high level synthesis systems and environments A reference text like this will allow the high level synthesis community to grow and prosper in the future

Customizable Embedded Processors Paolo Ienne,Rainer Leupers,2006-08-30 Customizable processors have been described as the next natural step in the evolution of the microprocessor business a step in the life of a new technology where top performance alone is no longer sufficient to guarantee market success Other factors become fundamental such as time to market convenience energy efficiency and ease of customization This book is the first to explore comprehensively one of the most fundamental trends which emerged in the last decade to treat processors not as rigid fixed entities which designers include as is in their products but rather to build sound methodologies to tailor fit processors to the specific needs of such products This book addresses the goal of maintaining a very large family of processors with a wide range of features at a cost comparable to that of maintaining a single processor First book to present comprehensively the major ASIP design methodologies and tools without any particular bias Written by most of the pioneers and top international experts of this young domain Unique mix of management perspective technical detail research outlook and practical implementation

*Logic and Architecture Synthesis* Gabriele Saucier,Anne Mignotte,2016-01-09 This book describes

several methods and systems solving one of the highlighted problems within computer aided design namely architectural and logic synthesis The book emphasises the most recent technologies in high level synthesis concentrating on applicative studies and practical constraints or criteria during synthesis Logic and Architecture Synthesis concentrates on the practical problems involving automatic synthesis of designs It is essential reading for researchers and CAD Managers working in this area

*Behavioral Synthesis for Hardware Security* Srinivas Katkoori, Sheikh Ariful Islam, 2022-02-08 This book presents state of the art research results from leading electronic design automation EDA researchers on automated approaches for generating cyber secure smart hardware The authors first provide brief background on high level synthesis principles and motivate the need for secure design during behavioral synthesis Then they provide readers with synthesis techniques for six automated security solutions namely hardware obfuscation hardware Trojan detection IP watermarking state encoding side channel attack resistance and information flow tracking Provides a single source reference to behavioral synthesis for hardware security Describes automatic synthesis techniques for algorithmic obfuscation using code transformations Includes behavioral synthesis techniques for intellectual property protection

**High-performance Bit-serial Datapath Implementation for Large- Scale Configurable Systems** Tsuyoshi Isshiki, 1996

**Finite State Machine Datapath Design, Optimization, and Implementation** Justin Davis, Robert Reese, 2022-05-31 Finite State Machine Datapath Design Optimization and Implementation explores the design space of combined FSM Datapath implementations The lecture starts by examining performance issues in digital systems such as clock skew and its effect on setup and hold time constraints and the use of pipelining for increasing system clock frequency This is followed by definitions for latency and throughput with associated resource tradeoffs explored in detail through the use of dataflow graphs and scheduling tables applied to examples taken from digital signal processing applications Also design issues relating to functionality interfacing and performance for different types of memories commonly found in ASICs and FPGAs such as FIFOs single ports and dual ports are examined Selected design examples are presented in implementation neutral Verilog code and block diagrams with associated design files available as downloads for both Altera Quartus and Xilinx Virtex FPGA platforms A working knowledge of Verilog logic synthesis and basic digital design techniques is required This lecture is suitable as a companion to the synthesis lecture titled Introduction to Logic Synthesis using Verilog HDL Table of Contents Calculating Maximum Clock Frequency Improving Design Performance Finite State Machine with Datapath FSM Design Embedded Memory Usage in Finite State Machine with Datapath FSM Designs

*Artificial Intelligence and Automation* Nikolaos G. Bourbakis, 1998

*Behavioral Synthesis and Component Reuse with VHDL* Ahmed Amine Jerraya, Hong Ding, Polen Kission, Maher Rahmouni, 2012-12-06 Improvement in the quality of integrated circuit designs and a designer's productivity can be achieved by a combination of two factors Using more structured design methodologies for extensive reuse of existing components and subsystems It seems that 70% of new designs correspond to existing components that cannot be reused because of a lack of

methodologies and tools Providing higher level design tools allowing to start from a higher level of abstraction After the success and the widespread acceptance of logic and RTL synthesis the next step is behavioral synthesis commonly called architectural or high level synthesis Behavioral Synthesis and Component Reuse with VHDL provides methods and techniques for VHDL based behavioral synthesis and component reuse The goal is to develop VHDL modeling strategies for emerging behavioral synthesis tools Special attention is given to structured and modular design methods allowing hierarchical behavioral specification and design reuse The goal of this book is not to discuss behavioral synthesis in general or to discuss a specific tool but to describe the specific issues related to behavioral synthesis of VHDL description This book targets designers who have to use behavioral synthesis tools or who wish to discover the real possibilities of this emerging technology The book will also be of interest to teachers and students interested to learn or to teach VHDL based behavioral synthesis

**Engineering of Intelligent Systems** Laszlo Monostori,Jozsef Vancza,Moonis Ali,2003-06-29 This book constitutes the refereed proceedings of the 14th International Conference on Industrial and Engineering Applications of Artificial Intelligence and Expert Systems IEA AIE 2001 held in Budapest Hungary in June 2001 The 104 papers presented were carefully reviewed and selected from a total of 140 submissions The proceedings offer topical sections on searching knowledge representation model based reasoning machine learning data mining soft computing evolutionary algorithms distributed problem solving expert systems pattern and speech recognition vision language processing planning and scheduling robotics autonomous agents design control manufacturing systems finance and business software engineering and intelligent tutoring

**Design and Implementation of High-level Synthesis of Pipelined Data-path and Clocking Scheme** Woohyun David Lee,1992 *Power Optimization and Synthesis at Behavioral and System Levels Using Formal Methods* Jui-Ming Chang,Massoud Pedram,2012-12-06 Integrated circuit densities and operating speeds continue to rise at an exponential rate Chips however cannot get larger and faster without a sharp decrease in power consumption beyond the current levels Minimization of power consumption in VLSI chips has thus become an important design objective In fact with the explosive growth in demand for portable electronics and the usual push toward more complex functionality and higher performance power consumption has in many cases become the limiting factor in satisfying the market demand A new generation of power conscious CAD tools are coming onto the market to help designers estimate optimize and verify power consumption levels at most stages of the IC design process These tools are especially prevalent at the register transfer level and below There is a great need for similar tools and capabilities at the behavioral and system levels of the design process Many researchers and CAD tool developers are working on high level power modeling and estimation as well as power constrained high level synthesis and optimization Techniques and tools alone are however insufficient to optimize VLSI circuit power dissipation a consistent and convergent design methodology is also required Power Optimization and Synthesis at Behavioral and System Levels Using Formal Methods was written to address some of the key problems in power analysis

and optimization early in the design process In particular this book focuses on power macro modeling based on regression analysis and power minimization through behavioral transformations scheduling resource assignment and hardware software partitioning and mapping What differentiates this book from other published work on the subject is the mathematical basis and formalism behind the algorithms and the optimality of these algorithms subject to the stated assumptions From the Foreword This book makes an important contribution to the field of system design technologies by presenting a set of algorithms with guaranteed optimality properties that can be readily applied to system level design This contribution is timely because it fills the need of new methods for a new design tool generation which supports the design of electronic systems with even more demanding requirements Giovanni De Micheli Professor Stanford University      *Compilation Techniques for Reconfigurable Architectures* João M.P. Cardoso, Pedro C. Diniz, 2011-04-02 The extreme exibility of reconfigurable architectures and their performance potential have made them a vehicle of choice in a wide range of computing domains from rapid circuit prototyping to high performance computing The increasing availability of transistors on a die has allowed the emergence of reconfigurable architectures with a large number of computing resources and interconnection topologies To exploit the potential of these reconfigurable architectures programmers are forced to map their applications typically written in high level imperative programming languages such as C or MATLAB to hardware oriented languages such as VHDL or Verilog In this process they must assume the role of hardware designers and software programmers and navigate a maze of program transformations mapping and synthesis steps to produce efficient reconfigurable computing implementations The richness and sophistication of any of these application mapping steps make the mapping of computations to these architectures an increasingly daunting process It is thus widely believed that automatic compilation from high level programming languages is the key to the success of reconfigurable computing This book describes a wide range of code transformations and mapping techniques for programs described in high level programming languages most notably imperative languages to reconfigurable architectures      *Image Processing Using FPGAs* Donald Bailey, 2019-06-11 This book presents a selection of papers representing current research on using field programmable gate arrays FPGAs for realising image processing algorithms These papers are reprints of papers selected for a Special Issue of the Journal of Imaging on image processing using FPGAs A diverse range of topics is covered including parallel soft processors memory management image filters segmentation clustering image analysis and image compression Applications include traffic sign recognition for autonomous driving cell detection for histopathology and video compression Collectively they represent the current state of the art on image processing using FPGAs      **Science Abstracts** ,1995      **A Designer's Guide to Asynchronous VLSI** Peter A. Beerel, Recep O. Ozdag, Marcos Ferretti, 2010-02-04 Create low power high performance circuits with shorter design times using this practical guide to asynchronous design This practical alternative to conventional synchronous design enables performance close to full custom designs with design times that approach commercially

available ASIC standard cell flows It includes design trade offs specific design examples and end of chapter exercises  
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