Tom Conte Nacho Navarro Wen-mei W. Hwu Mateo Valero Theo Ungerer (Eds.)

High Performance Embedded Architectures and Compilers

First International Conference, HiPEAC 2005 Barcelona, Spain, November 2005 Proceedings



Cristina Silvano, Koen Bertels, Michael Schulte

High Performance Embedded Architectures and Compilers Tom Conte, Nacho Navarro, Wen-mei W. Hwu, Mateo Valero, Theo Ungerer, 2005-10-27 As Chairmen of HiPEAC 2005 we have the pleasure of welcoming you to the proceedings of the rst international conference promoted by the HiPEAC N work of Excellence During the last year HiPEAC has been building its clusters of researchers in computer architecture and advanced compiler techniques for embedded and high performance computers Recently the Summer School has been the seed for a fruitful collaboration of renowned international faculty and young researchers from 23 countries with fresh new ideas Now the conference promises to be among the premier forums for discussion and debate on these research topics Theprestigeofasymposiumismainlydetermined by the quality of its tech cal program This rst programlived up to our high expectations thanks to the largenumber of strong submissions The ProgramCommittee received a total of 84 submissions only 17 were selected for presentation as full length papers and another one as an invited paper Each paper was rigorously reviewed by three ProgramCommittee members and at least one external referee Many reviewers spent a great amount of e ort to provide detailed feedback In many cases such feedback along with constructive shepherding resulted in dramatic improvement in the quality of accepted papers The names of the Program Committee m bers and the referees are listed in the proceedings. The net result of this team e ort is that the symposium proceedings include outstanding contributions by authors from nine countries in three continents In addition to paper presentations this rst HiPEAC conference featured two keynotes delivered by prominent researchers from industry and High Performance Embedded Architectures and Compilers Yale N. Patt, Pierfrancesco Foglia, Evelyn academia Duesterwald, Paolo Faraboschi, Xavier Martorell, 2010-01-21 This book constitutes the refereed proceedings of the 5th International Conference on High Performance Embedded Architectures and Compilers HiPEAC 2010 held in Pisa Italy in January 2010 The 23 revised full papers presented together with the abstracts of 2 invited keynote addresses were carefully reviewed and selected from 94 submissions The papers are organized in topical sections on architectural support for concurrency compilation and runtime systems reconfigurable and customized architectures multicore efficiency reliability and power memory organization and optimization and programming and analysis of accelerators **High Performance** and Embedded Architectures and Compilers Association for Computing Machinery, Manolis Katevenis, ACM Digital Library, Sigarch, Association for Computing Machinery. Special Interest Group on Embedded Systems, ACM Special Interest Group in Programming Languages, ACM Special Interest Group on Programming Languages, 2011 Transactions on High-Performance Embedded Architectures and Compilers IV Per Stenström, 2012-02-23 Transactions on HiPEAC aims at the timely dissemination of research contributions in computer architecture and compilation methods for high performance embedded computer systems Recognizing the convergence of embedded and general purpose computer systems this journal

publishes original research on systems targeted at specific computing tasks as well as systems with broad application bases The scope of the journal therefore covers all aspects of computer architecture code generation and compiler optimization methods of interest to researchers and practitioners designing future embedded systems This 4th issue contains 21 papers carefully reviewed and selected out of numerous submissions and is divided in four sections The first section contains five regular papers The second section consists of the top four papers from the 4th International Conference on High Performance Embedded Architectures and Compilers HiPEAC 2009 held in Paphos Cyprus in January 2009 The third section contains a set of six papers providing a snap shot from the Workshop on Software and Hardware Challenges of Manycore Platforms SHCMP 2008 held in Beijing China in June 2008 The fourth section consists of six papers from the 8th IEEE International Symposium on Systems Architectures Modeling and Simulation SAMOS VIII 2008 held in Samos Greece in July High Performance Embedded Architectures and Compilers André Seznec, Joel Emer, Michael O'Boyle, Margaret 2008 Martonosi, Theo Ungerer, 2008-12-24 This book constitutes the refereed proceedings of the Fourth International Conference on High Performance Embedded Architectures and Compilers HiPEAC 2009 held in Paphos Cyprus in January 2009 The 27 revised full papers presented together with 2 invited keynote paper were carefully reviewed and selected from 97 submissions. The papers are organized in topical sections on dynamic translation and optimisation low level scheduling parallelism and resource control communication mapping for CMPs power cache issues as well as parallel embedded applications High Performance Embedded Architectures and Compilers Koen De Bosschere, David Kaeli, Per Stenström, David Whalley, Theo Ungerer, 2007-07-20 This book constitutes the refereed proceedings of the Second International Conference on High Performance Embedded Architectures and Compilers HiPEAC 2007 held in Ghent Belgium in January 2007 The 19 revised full papers presented together with one invited keynote paper were carefully reviewed and selected from 65 submissions The papers are organized in topical sections High Performance Embedded Architectures and Compilers Per Stenström, Michel Dubois, Manolis Katevenis, Rajiv Gupta, Theo Ungerer, 2008-01-18 This highly relevant and up to the minute book constitutes the refereed proceedings of the Third International Conference on High Performance Embedded Architectures and Compilers HiPEAC 2008 held in G teborg Sweden January 27 29 2008 The 25 revised full papers presented together with 1 invited keynote paper were carefully reviewed and selected from 77 submissions The papers are organized into topical sections on a number of key subjects in the field Transactions on High-Performance Embedded Architectures and Compilers III Per Stenström, 2011-02-23 Transactions on HiPEAC aims at the timely dissemination of research contributions in computer architecture and compilation methods for high performance embedded computer systems Recognizing the convergence of embedded and general purpose computer systems this journal publishes original research on systems targeted at specific computing tasks as well as systems with broad application bases. The scope of the journal therefore covers all aspects of computer architecture code generation and compiler optimization methods of

interest to researchers and practitioners designing future embedded systems. This third issue contains 14 papers carefully reviewed and selected out of numerous submissions and is divided into four sections. The first section contains the top four papers from the Third International Conference on High Performance Embedded Architectures and Compilers HiPEAC 2008 held in G teborg Sweden in January 2008 The second section consists of four papers from the 8th MEDEA Workshop held in conjunction with PACT 2007 in Brasov Romania in September 2007 The third section contains two regular papers and the fourth section provides a snapshot from the First Workshop on Programmability Issues for Multicore Computers MULTIPROG **Transactions on High-Performance Embedded Architectures and** held in conjunction with HiPEAC 2008 Compilers V Cristina Silvano, Koen Bertels, Michael Schulte, 2019-02-22 Transactions on HiPEAC aims at the timely dissemination of research contributions in computer architecture and compilation methods for high performance embedded computer systems Recognizing the convergence of embedded and general purpose computer systems this journal publishes original research on systems targeted at specific computing tasks as well as systems with broad application bases The scope of the journal therefore covers all aspects of computer architecture code generation and compiler optimization methods of interest to researchers and practitioners designing future embedded systems This 5th issue contains extended versions of papers by the best paper award candidates of IC SAMOS 2009 and the SAMOS 2009 Workshop colocated events of the 9th International Symposium on Systems Architectures Modeling and Simulation SAMOS 2009 held in Samos Greece in 2009 The 7 papers included in this volume were carefully reviewed and selected. The papers cover research on embedded processor hardware software design and integration and present challenging research trends **Transactions on** High-Performance Embedded Architectures and Compilers II Per Stenström, David Whalley, 2009-04-22 This book contains extended versions of key papers from the 2nd International Conference on High Performance Embedded Architectures and Compilers HiPEAC 2007 It also covers such topics as microarchitecture code generation and performance modeling Transactions on High-Performance Embedded Architectures and Compilers II Per Stenström, David Whalley, 2009-04-22 This book contains extended versions of key papers from the 2nd International Conference on High Performance Embedded Architectures and Compilers HiPEAC 2007 It also covers such topics as microarchitecture code generation and performance modeling CASES 2005: International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, September 24-27, 2005, San Francisco, California, USA. International Conference on Compilers, Architectures and Synthesis for Embedded Systems, 2005 4th International Conference on High-performance and *Embedded Architectures and Compilers* ,2011 High Performance Embedded Architectures and Compilers André Transactions on High-Performance Embedded Architectures and Compilers I Mike O'Boyle, Francois Seznec,2009 Bodin, Marcelo Cintra, Sally A. McKee, 2007-04-13 Transactions on HiPEAC is a new journal which aims at the timely dissemination of research contributions in computer architecture and compilation methods for high performance embedded

computer systems It publishes original research on systems targeted at specific computing tasks as well as systems with broad application bases Its scope covers all aspects of computer architecture code generation and compiler optimization methods Proceedings of the 6th International Conference on High Performance and Embedded Architectures and Compilers Association for Computing Machinery, ACM Digital Library, 2011 HIPEAC '11: Proceedings of the 6th International Conference on High Performance and Embedded Architectures and Compilers, 24-26 January 2011, Heraklion, Grete, Greece Manolis Katevenis, 2011 *Embedded Computer Systems: Architectures, Modeling, and Simulation Timo D.* Hämäläinen, 2005-07-04 This book constitutes the refereed proceedings of the 5th International Workshop on Systems Architectures Modeling and Simulation SAMOS 2005 held in Samos Greece in July 2005 The 49 revised full papers presented were thoroughly reviewed and selected from 114 submissions. The papers are organized in topical sections on reconfigurable system design and implementations processor architectures design and simulation architectures and implementations system level design and modeling and simulation Embedded Software and Systems Zhaohui Wu, Minyi Guo, Chun Chen, Jiajun Bu, 2005-08-29 Welcome to the post proceedings of the First International Conference on Embedded Software and Systems ICESS 2004 which was held in Hangzhou P R China 9 10 December 2004 Embedded Software and Systems technology is of increasing importance for a wide range of industrial areas such as aerospace automotive telecommunication and manufacturing automation Embedded technology is playing an increasingly dominant role in modern society This is a natural outcome of amazingly fast developments in the embedded field The ICESS 2004 conference brought together researchers and developers from academia industry and government to advance the science engineering and technology in embedded software and systems development and provided them with a forum to present and exchange their ideas results work in progress and experience in all areas of embedded systems research and development The ICESS 2004 conference attracted much more interest than expected The total number of paper submissions to the main conference and its three workshops namely Pervasive Computing Automobile Electronics and Tele communication was almost 400 from nearly 20 countries and regions All submissions were reviewed by at least three Program or Technical Committee members or external reviewers It was extremely difficult to make the final decision on paper acceptance because there were so many excellent foreseeing and interesting submissions with brilliant ideas Embedded Software and Systems Laurence T. Yang, 2005-12-05 This book constitutes the refereed proceedings of the Second International Conference on Embedded Software and Systems ICESS 2005 held in Xi an China in December 2005 The 63 revised full papers presented together with the abstracts of 3 keynote speeches were thoroughly reviewed and selected from 361 submissions. The papers are organized in topical sections on embedded hardware embedded software real time systems power aware computing hardware software co design and system on chip testing and verification reconfigurable computing agent and distributed computing wireless communications mobile computing pervasive ubiquitous computing and intelligence multimedia and human computer interaction network protocol

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