Fault Covering Problems in Reconfigurable VLSI Systems

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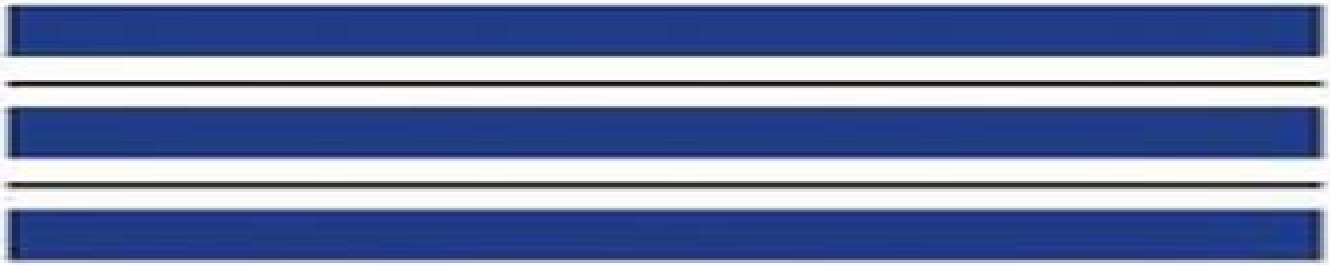

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Fault Covering Problems In Reconfigurable Vlsi Systems

Israel Koren

Fault Covering Problems In Reconfigurable Vlsi Systems:

Fault Covering Problems in Reconfigurable VLSI Systems Ran Libeskind-Hadas,Nany Hasan,Jingsheng Jason Cong,Philip McKinley,C.L. Liu,2012-12-06 Fault Covering Problems in Reconfigurable VLSI Systems describes the authors recent research on reconfiguration problems for fault tolerance in VLSI and WSI Systems The book examines solutions to a number of reconfiguration problems Efficient algorithms are given for tractable covering problems and general techniques are given for dealing with a large number of intractable covering problems The book begins with an investigation of algorithms for the reconfiguration of large redundant memories Next a number of more general covering problems are considered and the complexity of these problems is analyzed Finally a general and uniform approach is proposed for solving a wide class of covering problems The results and techniques described here will be useful to researchers and students working in this area As such the book serves as an excellent reference and may be used as the text for an advanced course on the topic **Defect and Fault Tolerance in VLSI Systems** Israel Koren,2012-12-06 This book contains an edited selection of papers presented at the International Workshop on Defect and Fault Tolerance in VLSI Systems held October 6 7 1988 in Springfield Massachusetts Our thanks go to all the contributors and especially the members of the program committee for the difficult and time consuming work involved in selecting the papers that were presented in the workshop and reviewing the papers included in this book Thanks are also due to the IEEE Computer Society in particular the Technical Committee on Fault Tolerant Computing and the Technical Committee on VLSI and the University of Massachusetts at Amherst for sponsoring the workshop and to the National Science Foundation for supporting under grant number MIP 8803418 the keynote address and the distribution of this book to all workshop attendees The objective of the workshop was to bring t ogether researchers and practition ers from both industry and academia in the field of defect tolerance and yield en ha ncement in VLSI to discuss their mutual interests in defect tolerant architectures and models for integrated circuit defects faults and yield Progress in this area was slowed down by the proprietary nature of yield related data and by the lack of appropriate forums for disseminating such information The goal of this workshop was therefore to provide a forum for a dialogue and exchange of views A follow up workshop in October 1989 with C H Stapper from IBM and V K Jain from the University of South Florida as general co chairmen is being organized Defect and Fault Tolerance in VLSI Systems C.H. Stapper,V.K. Jain,Gabriele Saucier,2013-06-29 Higher circuit densities increasingly more complex application ohjectives and advanced packaging technologies have suhstantially increased the need to incorporate defect tolerance and fault tolerance in the design of VLSI and WSI systems The goals of defect tolerance and fault tolerance are yield enhancement and improved reliahility The emphasis on this area has resulted in a new field of interdisciplinary scientific research I n fact advanced methods of defect fault control and tolerance are resulting in enhanced manufacturahility and productivity of integrated circuit chips VI SI systems and wafer scale integrated circuits In 1987 Dr W Moore organized an International Workshop on

Designing for Yield at Oxford University Edited papers of that workshop were published in reference II The participants in that workshop agreed that meetings of this type should he con tinued preferahly on a yearly hasis It was Dr I Koren who organized the IEEE Inter national Workshop on Defect and Fault Tolerance in VLSI Systems in Springfield Massachusetts the next year Selected papers from that workshop were puhlished as the first volume of this series 21 *Reconfiguration of Fault Tolerant VLSI Systems* Ran Libeskind-Hadas,Ran Hadas-Libeskind,University of Illinois at Urbana-Champaign. Department of Computer Science,1993 For the NP hard reconfiguration problems we propose several strategies For some problems polynomial time approximation algorithms are presented that yield provably good but not necessarily optimal solutions For some reconfiguration problems however approximation algorithms are not meaningful For these problems effective search strategies and heuristics are proposed *High Level Synthesis of ASICs under Timing and Synchronization Constraints* David C. Ku,Giovanni DeMicheli,2013-03-14 Computer aided synthesis of digital circuits from behavioral level specifications offers an effective means to deal with increasing complexity of digital hardware design High Level Synthesis of ASICs Under Timing and Synchronization Constraints addresses both theoretical and practical aspects in the design of a high level synthesis system that transforms a behavioral level description of hardware to a synchronous logic level implementation consisting of logic gates and registers High Level Synthesis of ASICs Under Timing and Synchronization Constraints addresses specific issues in applying high level synthesis techniques to the design of ASICs This complements previous results achieved in synthesis of general purpose and signal processors where data path design is of utmost importance In contrast ASIC designs are often characterized by complex control schemes to support communication and synchronization with the environment The combined design of efficient data path control unit is the major contribution of this book Three requirements are important in modeling ASIC designs concurrency external synchronization and detailed timing constraints The objective of the research work presented here is to develop a hardware model incorporating these requirements as well as synthesis algorithms that operate on this hardware model The contributions of this book address both the theory and the implementation of algorithm for hardware synthesis *The SECD Microprocessor* Brian T. Graham,2012-12-06 This is a milestone in machine assisted microprocessor verification Gordon 20 and Hunt 32 led the way with their verifications of sim ple designs Cohn 12 13 followed this with the verification of parts of the VIPER microprocessor This work illustrates how much these and other pioneers achieved in developing tractable models scalable tools and a robust methodology A condensed review of previous re search emphasising the behavioural model underlying this style of verification is followed by a careful and remarkably readable ac count of the SECD architecture its formalisation and a report on the organisation and execution of the automated correctness proof in HOL This monograph reports on Graham s MSc project demonstrat ing that in the right hands the tools and methodology for formal verification can and therefore should now be applied by someone with little previous expertise in formal methods to verify a non trivial microprocessor in a limited timescale This is not to

belittle Graham s achievement the production of this proof work ing as Graham did from the previous literature goes well beyond a typical MSc project The achievement is that with this exposition to hand an engineer tackling the verification of similar microprocessor designs will have a clear view of the milestones that must be passed on the way and of the methods to be applied to achieve them **Field-Programmable Gate Arrays** Stephen D. Brown,Robert J. Francis,Jonathan Rose,Zvonko G. Vranesic,2012-12-06 Field Programmable Gate Arrays FPGAs have emerged as an attractive means of implementing logic circuits providing instant manufacturing turnaround and negligible prototype costs They hold the promise of replacing much of the VLSI market now held by mask programmed gate arrays FPGAs offer an affordable solution for customized VLSI over a wide variety of applications and have also opened up new possibilities in designing reconfigurable digital systems Field Programmable Gate Arrays discusses the most important aspects of FPGAs in a textbook manner It provides the reader with a focused view of the key issues using a consistent notation and style of presentation It provides detailed descriptions of commercially available FPGAs and an in depth treatment of the FPGA architecture and CAD issues that are the subjects of current research The material presented is of interest to a variety of readers including those who are not familiar with FPGA technology but wish to be introduced to it as well as those who already have an understanding of FPGAs but who are interested in learning about the research directions that are of current interest *Electronic CAD Frameworks* Timothy J. Barnes,David Harrison,A. Richard Newton,Rick L. Spickelmier,2012-12-06 When it comes to frameworks the familiar story of the elephant and the six blind philosophers seems to apply As each philoso pher encountered a separate part of the elephant each pronounced his considered but flawed judgement One blind philosopher felt a leg and thought it a tree Another felt the tail and thought he held a rope Another felt the elephant s flank and thought he stood before a wall We re supposed to learn about snap judgements from this alle gory but its author might well have been describing design automation frameworks For in the reality of today s product development requirements a framework must be many things to many people xiv CAD Frameworks Integration Technology for CAD As the authors of this book note framework design is an optimi zation problem Somehow it has to be both a superior rope for one and a tremendous tree for another Somehow it needs to provide a standard environment for exploiting the full potential of computer aided engineering tools And somehow it has to make real such abstractions as interoperability and interchangeability For years we ve talked about a framework as something that provides application oriented services just as an operating system provides system level support And for years that simple statement has hid the tremendous complexity of actually providing those services

Anatomy of a Silicon Compiler Robert W. Brodersen,2012-12-06 A silicon compiler is a software system which can automatically generate an integrated circuit from a user s specification Anatomy of a Silicon Compiler examines one such compiler in detail covering the basic framework and design entry the actual algorithms and libraries which are used the approach to verification and testing behavioral synthesis tools and several applications which demonstrate the system s

capabilities Hot-Carrier Reliability of MOS VLSI Circuits Yusuf Leblebici,Sung-Mo (Steve) Kang,2012-12-06 As the complexity and the density of VLSI chips increase with shrinking design rules the evaluation of long term reliability of MOS VLSI circuits is becoming an important problem The assessment and improvement of reliability on the circuit level should be based on both the failure mode analysis and the basic understanding of the physical failure mechanisms observed in integrated circuits Hot carrier induced degrada tion of MOS transistor characteristics is one of the primary mechanisms affecting the long term reliability of MOS VLSI circuits It is likely to become even more important in future generation chips since the down ward scaling of transistor dimensions without proportional scaling of the operating voltage aggravates this problem A thorough understanding of the physical mechanisms leading to hot carrier related degradation of MOS transistors is a prerequisite for accurate circuit reliability evaluation It is also being recognized that important reliability concerns other than the post manufacture reliability qualification need to be addressed rigorously early in the design phase The development and use of accurate reliability simulation tools are therefore crucial for early assessment and improvement of circuit reliability Once the long term reliability of the circuit is estimated through simulation the results can be compared with predetermined reliability specifications or limits If the predicted reliability does not satisfy the requirements appropriate design modifications may be carried out to improve the resistance of the devices to degradation Design Automation for Timing-Driven Layout Synthesis S. Sapatnekar,Sung-Mo (Steve) Kang,2012-12-06 Moore s law Noy77 which predicted that the number of devices in tegrated on a chip would be doubled every two years was accurate for a number of years Only recently has the level of integration be gun to slow down somewhat due to the physical limits of integration technology Advances in silicon technology have allowed Ie design ers to integrate more than a few million transistors on a chip even a whole system of moderate complexity can now be implemented on a single chip To keep pace with the increasing complexity in very large scale integrated VLSI circuits the productivity of chip designers would have to increase at the same rate as the level of integration Without such an increase in productivity the design of complex systems might not be achievable within a reasonable time frame The rapidly increasing complexity of VLSI circuits has made de 1 2 INTRODUCTION sign automation an absolute necessity since the required increase in productivity can only be accomplished with the use of sophisticated design tools Such tools also enable designers to perform trade off analyses of different logic implementations and to make well informed design decisions Digital BiCMOS Integrated Circuit Design Sherif H.K. Embabi,Abdellatif Bellaouar,Mohamed I. Elmasry,2012-12-06 Digital BiCMOS Integrated Circuit Design is the first book devoted entirely to the analysis and design of digital BiCMOS integrated circuits BiCMOS Integrated Circuit Design also reviews CMOS and CML integrated circuit design The application of BiCMOS in the design of digital subsystems e g adders multipliers RAMs and PLAs is addressed The book also introduces the reader to IC process technology CMOS bipolar and BiCMOS The modeling of both the bipolar and MOS devices are covered Many process device circuit design issues are discussed Digital BiCMOS

Integrated Circuit Design can be used by engineers researchers graduate and senior undergraduate students working in the area of digital integrated circuits digital circuits and system design BiCMOS process and device modeling **Wavelet Theory and Its Applications** Randy K. Young,2012-12-06 The continuous wavelet transform has deep mathematical roots in the work of Alberto P Calderon His seminal paper on complex method of interpolation and intermediate spaces provided the main tool for describing function spaces and their approximation properties The Calderon identities allow one to give integral representations of many natural operators by using simple pieces of such operators which are more suited for analysis These pieces which are essentially spectral projections can be chosen in clever ways and have proved to be of tremendous utility in various problems of numerical analysis multidimensional signal processing video data compression and reconstruction of high resolution images and high quality speech A proliferation of research papers and a couple of books written in English there is an earlier book written in French have emerged on the subject These books so far are written by specialists for specialists with a heavy mathematical flavor which is characteristic of the Calderon Zygmund theory and related research of Duffin Schaeffer Daubechies Grossman Meyer Morlet Chui and others Randy Young s monograph is geared more towards practitioners and even non specialists who want and probably should be cognizant of the exciting proven as well as potential benefits which have either already emerged or are likely to emerge from wavelet theory **Acoustical and Environmental Robustness in Automatic Speech Recognition** A. Acero,2012-12-06 The need for automatic speech recognition systems to be robust with respect to changes in their acoustical environment has become more widely appreciated in recent years as more systems are finding their way into practical applications Although the issue of environmental robustness has received only a small fraction of the attention devoted to speaker independence even speech recognition systems that are designed to be speaker independent frequently perform very poorly when they are tested using a different type of microphone or acoustical environment from the one with which they were trained The use of microphones other than a close talking headset also tends to severely degrade speech recognition performance Even in relatively quiet office environments speech is degraded by additive noise from fans slamming doors and other conversations as well as by the effects of unknown linear filtering arising reverberation from surface reflections in a room or spectral shaping by microphones or the vocal tracts of individual speakers Speech recognition systems designed for long distance telephone lines or applications deployed in more adverse acoustical environments such as motor vehicles factory floors oroutdoors demand far greaterdegrees ofenvironmental robustness There are several different ways of building acoustical robustness into speech recognition systems Arrays of microphones can be used to develop a directionally sensitive system that resists intelference from competing talkers and other noise sources that are spatially separated from the source of the desired speech signal

Algorithms for Synthesis and Testing of Asynchronous Circuits Luciano Lavagno,Alberto L. Sangiovanni-Vincentelli,2012-12-06 Since the second half of the 1980s asynchronous circuits have been the subject of a great

deal of research following a period of relative oblivion The lack of interest in asynchronous techniques was motivated by the progressive shift towards synchronous design techniques that had much more structure and were much easier to verify and synthesize System design requirements made it impossible to eliminate totally the use of asynchronous circuits Given the objective difficulty encountered by designers the asynchronous components of electronic systems such as interfaces became a serious bottleneck in the design process The use of new models and some theoretical breakthroughs made it possible to develop asynchronous design techniques that were reliable and effective This book describes a variety of mathematical models and of algorithms that form the backbone and the body of a new design methodology for asyn chronous design The book is intended for asynchronous hardware designers for computer aided tool experts and for digital designers interested in ex ploring the possibility of designing asynchronous circuits It requires a solid mathematical background in discrete event systems and algorithms While the book has not been written as a textbook nevertheless it could be used as a reference book in an advanced course in logic synthesis or asynchronous design **Encyclopedia of Computer Science and Technology** Allen Kent,James G. Williams,1995-02-14 Compiler Construction to Visualization and Quantification of Vortex Dominated Flows Logic Synthesis and Optimization Tsutomu Sasao,2012-12-06 Logic Synthesis and Optimization presents up to date research information in a pedagogical form The authors are recognized as the leading experts on the subject The focus of the book is on logic minimization and includes such topics as two level minimization multi level minimization application of binary decision diagrams delay optimization asynchronous circuits spectral method for logic design field programmable gate array FPGA design EXOR logic synthesis and technology mapping Examples and illustrations are included so that each contribution can be read independently Logic Synthesis and Optimization is an indispensable reference for academic researchers as well as professional CAD engineers **High-Level Synthesis for Real-Time Digital Signal Processing** Jan Vanhoof,Karl Van Rompaey,Ivo Bolsens,Gert Goossens,Hugo De Man,2012-12-06 High Level Synthesis for Real Time Digital Signal Processing is a comprehensive reference work for researchers and practicing ASIC design engineers It focuses on methods for compiling complex low to medium throughput DSP system and on the implementation of these methods in the CATHEDRAL II compiler The emergence of independent silicon foundries the reduced price of silicon real estate and the shortened processing turn around time bring silicon technology within reach of system houses Even for low volumes digital systems on application specific integrated circuits ASICs are becoming an economically meaningful alternative for traditional boards with analogue and digital commodity chips ASICs cover the application region where inefficiencies inherent to general purpose components cannot be tolerated However full custom handcrafted ASIC design is often not affordable in this competitive market Long design times a high development cost for alow production volume the lack of silicon designers and the lack of suited design facilities are inherent difficulties to manual full custom chip design To overcome these drawbacks complex systems have to be integrated in ASICs much faster and without losing too much efficiency in silicon area and

operation speed compared to handcrafted chips The gap between system design and silicon design can only be bridged by new design CAD The idea of a silicon compiler translating a behavioural system specification directly into silicon was born from the awareness that the ability to fabricate chips is indeed outrunning the ability to design them At this moment CAD is one order of magnitude behind schedule Conceptual CAD is the keyword to mastering the design complexity in ASIC design and the topic of this book **Sigma Delta Modulators** Søren Hein,Avideh Zakhor,2012-12-06 Analog to digital A D converters are key components in digital signal processing DSP systems and are therefore receiving much attention as DSP becomes increasingly prevalent in telephony audio video consumer products etc The varying demands on conversion rate resolution and other characteristics have inspired a large number of competing A D conversion techniques Sigma Delta Modulators Nonlinear Decoding Algorithms and Stability Analysis is concerned with the particular class of A D techniques called oversampled noise shaping ONS that has recently come into prominence for a number of applications The popularity of ONS converters is due to their ease of implementation and robustness to circuit imperfectors An ONS converter consists of an encoder that generates a high rate low resolution digital signal and a decoder that produces a low rate high resolution digital approximation to the analog encoder input The conventional decoding approach is based on linear filtering Sigma Delta Modulators presents the optimal design of an ONS decoder for a given encoder It is shown that nonlinear decoding can achieve gains in signaling ratio and the encoder architecture The book then addresses the instability problem that plagues higher order ONS encoders A new stability concept is introduced that is well suited to ONS encoders and it is applied to the double loop encoder as well as to the class of interpolative encoders It is shown that there exists a trade off between stability and SNR performance Based on the results explicit design examples are presented Sigma Delta Modulators Nonlinear Decoding Algorithms and Stability Analysis is a valuable reference source for researchers and engineers in industry and academia working on or interested in design and analysis of A D converters particularly to those working in quantization theory and signal reconstruction and can serve as a text for advanced courses on the subjects treated *Motion Analysis and Image Sequence Processing* M. Ibrahim Sezan,Reginald L. Lagendijk,2012-12-06 An image or video sequence is a series of two dimensional 2 D images sequen tially ordered in time Image sequences can be acquired for instance by video motion picture X ray or acoustic cameras or they can be synthetically gen erated by sequentially ordering 2 D still images as in computer graphics and animation The use of image sequences in areas such as entertainment visual communications multimedia education medicine surveillance remote control and scientific research is constantly growing as the use of television and video systems are becoming more and more common The boosted interest in digital video for both consumer and professional products along with the availability of fast processors and memory at reasonable costs has been a major driving force behind this growth Before we elaborate on the two major terms that appear in the title of this book namely motion analysis and image sequence processing we like to place them in their proper contexts within the range of possible

operations that involve image sequences In this book we choose to classify these operations into three major categories namely i image sequence processing ii image sequence analysis and iii visualization The interrelationship among these three categories is pictorially described in Figure 1 below in the form of an image sequence triangle

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