

Formal Verification

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graph TD; A[Formal Verification] --> B[Model Checking]; A --> C[Theorem Proving]; A --> D[Equivalence Checking]; D --> E[Combinational]; D --> F[Sequential];
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Formal Methods For Vlsi Design

Laurence Pierre, Thomas Kropf



Formal Methods For Vlsi Design:

Formal Methods for VLSI Design Jørgen Staunstrup, 1990 These lecture notes contain an overview of an exciting new field of research formal methods which give the VLSI designer a firm foundation and useful tools for developing integrated circuits Such methods allow the possibility of systematic verification in the early phases of the design process By verifying high level descriptions of the design before concerning themselves with low level details designers can avoid wasting time implementing circuits that would later be discarded Obviously it can be very expensive to locate and correct errors found in the later stages of a project especially if correcting these errors requires extensive global changes to the design Furthermore the long turn around time for circuit fabrication makes it attractive to use techniques which uncover errors at an early phase of the design The summer school where these lectures were given was held in Denmark in June 1990 and consisted of six series of lectures each presenting a distinct formal method Formal Methods for VLSI Design J. Staunstrup, 1989

Formal Methods for VLSI Design Simon Read, 1994 Applying Formal Methods to Representation of Constraints in VLSI Design Specification Liming Cai, 1994 **Correct Hardware Design and Verification Methods** Laurence Pierre, Thomas Kropf, 2003-07-31 CHARME 99 is the tenth in a series of working conferences devoted to the development and use of leading edge formal techniques and tools for the design and verification of hardware and systems Previous conferences have been held in Darmstadt 1984 Edinburgh 1985 Grenoble 1986 Glasgow 1988 Leuven 1989 Torino 1991 Arles 1993 Frankfurt 1995 and Montreal 1997 This workshop and conference series has been organized in cooperation with IFIP WG 10.5 It is now the biannual counterpart of FMCAD which takes place every even numbered year in the USA The 1999 event took place in Bad Herrenalb a resort village located in the Black Forest close to the city of Karlsruhe The validation of functional and timing behavior is a major bottleneck in current VLSI design systems A predominantly academic area of study until a few years ago formal design and verification techniques are now migrating into industrial use The aim of CHARME 99 is to bring together researchers and users from academia and industry working in this active area of research Two invited talks illustrate major current trends the presentation by Gerard Berry Ecole des Mines de Paris Sophia Antipolis France is concerned with the use of synchronous languages in circuit design and the talk given by Peter Jansen BMW Munich Germany demonstrates an application of formal methods in an industrial environment The program also includes 20 regular presentations and 12 short presentations poster exhibitions that have been selected from the 48 submitted papers

Applied Formal Methods for Correct VLSI Design Luc J.M. Claesen, IMEC-IFIP International Workshop on Applied Formal Methods for Correct VLSI Design, 1989 **Correct Hardware Design and Verification Methods** Daniel Geist, Enrico Tronci, 2003-10-10 This book constitutes the refereed proceedings of the 12th IFIP WG 10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods CHARME 2003 held in L'Aquila Italy in October 2003 The 24 revised full papers and 8 short papers presented were carefully reviewed and selected from 65 submissions The papers

are organized in topical sections on software verification automata based methods processor verification specification methods theorem proving bounded model checking and model checking and applications *Correct Hardware Design and Verification Methods* George J. Milne, Laurence Pierre, 1993-05-12 These proceedings contain the papers presented at the Advanced Research Working Conference on Correct Hardware Design Methodologies held in Arles France in May 1993 and organized by the ESPRIT Working Group 6018 CHARME 2 and the Universit de Provence Marseille in cooperation with IFIP Working Group 10.2 Formal verification is emerging as a plausible alternative to exhaustive simulation for establishing correct digital hardware designs The validation of functional and timing behavior is a major bottleneck in current VLSI design systems slowing the arrival of products in the marketplace with its associated increase in cost From being a predominantly academic area of study until a few years ago formal design and verification techniques are now beginning to migrate into industrial use As we are now witnessing an increase in activity in this area in both academia and industry the aim of this working conference was to bring together researchers and users from both communities Formal VLSI Specification and Synthesis Luc J. M. Claesen, 1990 Functional and behavioral verification of correctness forms the bottleneck in current VLSI design systems For economical reasons design of VLSI circuits must be completely validated before manufacturing Current VLSI validation is mainly done through extensive simulation The emerging alternative is based on formal design and verification methods that guarantee correctness This book describes original work in all aspects of formal hardware design methods Topics covered include high level specification hardware description languages formal hardware verification methods guided synthesis methods correctness preserving transformations use of theorem provers for verification formal proof of correctness MOS timing verification methods design for verifiability and practical experiences

Correct Hardware Design and Verification Methods Tiziana Margaria, Tiziana Margaria-Steffen, Tom F. Melham, 2001-08-27 This book constitutes the refereed proceedings of the 11th IFIP WG 10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods CHARME 2001 held in Livingston Scotland UK in September 2001 The 28 revised full papers and eight short papers presented together with two invited papers and one special paper were carefully reviewed and selected from 56 submissions The book offers topical sections on model checking clocking issues theorem proving with higher order logics hardware compilation tools component verification case studies algorithm verification and duration calculus **Theorem Provers in Circuit Design** Ramayya Kumar, Thomas Kropf, 1995-03-06 This two volume set contains papers presented at the International Conference on Computational Engineering Science ICES 95 held in Mauna Lani Hawaii from 30 July to 3 August 1995 The contributions capture the state of the science in computational modeling and simulation in a variety of engineering disciplines civil mechanical aerospace materials and electronics engineering Applied Formal Methods for Correct VLSI Design, 1990 **System-on-Chip Methodologies & Design Languages** Peter J. Ashenden, Jean Mermet, Ralf Seepold, 2013-03-14 System on Chip

Methodologies the Forum on Design Languages FDL held in Europe and the Asia Pacific Chip Design Language APChDL Conference The papers cover a range of topics including design methods specification and modeling languages tool issues formal verification simulation and synthesis The results presented in these papers will help researchers and practicing engineers keep abreast of developments in this rapidly evolving field

Higher Order Logic Theorem Proving and Its Applications Jeffrey J. Joyce, Carl-Johan H. Seger, 1994-04-28 This volume constitutes the refereed proceedings of the 1993 Higher Order Logic User's Group Workshop held at the University of British Columbia in August 1993 The workshop was sponsored by the Centre for Integrated Computer System Research It was the sixth in the series of annual international workshops dedicated to the topic of Higher Order Logic theorem proving its usage in the HOL system and its applications The volume contains 40 papers including an invited paper by David Parnas McMaster University Canada entitled Some theorems we should prove

Higher Order Logic Theorem Proving and Its Applications Thomas F. Melham, 1994-09-07 This volume presents the proceedings of the 7th International Workshop on Higher Order Logic Theorem Proving and Its Applications held in Valetta Malta in September 1994 Besides 3 invited papers the proceedings contains 27 refereed papers selected from 42 submissions In total the book presents many new results by leading researchers working on the design and applications of theorem provers for higher order logic In particular this book gives a thorough state of the art report on applications of the HOL system one of the most widely used theorem provers for higher order logic

Electronic Design Automation for IC System Design, Verification, and Testing Luciano Lavagno, Igor L. Markov, Grant Martin, Louis K. Scheffer, 2017-12-19 The first of two volumes in the Electronic Design Automation for Integrated Circuits Handbook Second Edition Electronic Design Automation for IC System Design Verification and Testing thoroughly examines system level design microarchitectural design logic verification and testing Chapters contributed by leading experts authoritatively discuss processor modeling and design tools using performance metrics to select microprocessor cores for integrated circuit IC designs design and verification languages digital simulation hardware acceleration and emulation and much more New to This Edition Major updates appearing in the initial phases of the design flow where the level of abstraction keeps rising to support more functionality with lower non recurring engineering NRE costs Significant revisions reflected in the final phases of the design flow where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting edge applications and approaches realized in the decade since publication of the previous edition these are illustrated by new chapters on high level synthesis system on chip SoC block based design and back annotating system level models Offering improved depth and modernity Electronic Design Automation for IC System Design Verification and Testing provides a valuable state of the art reference for electronic design automation EDA students researchers and professionals

Theorem Proving in Higher Order Logics Jim Grundy, Malcolm Newey, 1998-09-09 This book constitutes the refereed proceedings of the 11th International Conference on Theorem Proving

in Higher Order Logics TPHOLs 98 held in Canberra Australia in September October 1998 The 26 revised full papers presented were carefully reviewed and selected from a total of 52 submissions Also included are two invited papers The papers address all current aspects of theorem proving in higher order logics and formal verification and program analysis Besides the HOL system the theorem provers Coq Isabelle LAMBDA LEGO NuPrl and PVS are discussed

Fundamentals and Standards in Hardware Description Languages Jean Mermet, 2012-12-06 The second half of this century will remain as the era of proliferation of electronic computers They did exist before but they were mechanical During next century they may perform other mutations to become optical or molecular or even biological Actually all these aspects are only fancy dresses put on mathematical machines This was always recognized to be true in the domain of software where machine or high level languages are more or less rigorous but immaterial variations of the universally accepted mathematical language aimed at specifying elementary operations functions algorithms and processes But even a mathematical machine needs a physical support and this is what hardware is all about The invention of hardware description languages HDLs in the early 60s was an attempt to stay longer at an abstract level in the design process and to push the stage of physical implementation up to the moment when no more technology independent decisions can be taken It was also an answer to the continuous exponential growth of complexity of systems to be designed This problem is common to hardware and software and may explain why the syntax of hardware description languages has followed with a reasonable delay of ten years the evolution of the programming languages at the end of the 60s they were Algol like a decade later Pascal like and now they are C or ADA like They have also integrated the new concepts of advanced software specification languages

Tools and Algorithms for the Construction and Analysis of Systems Hubert Garavel, John Hatcliff, 2003-07-01 This book constitutes the refereed proceedings of the 9th International Conference on Tools and Algorithms for the Construction and Analysis of Systems TACAS 2003 held in Warsaw Poland in April 2003 The 43 revised full papers presented were carefully reviewed and selected from 160 submissions The papers are organized in topical sections on bounded model checking and SAT based methods mu calculus and temporal logics verification of parameterized systems abstractions and counterexamples real time and scheduling security and cryptography modules and compositional verification symbolic state spaces and decision diagrams performance and mobility state space reductions constraint solving and decision procedures and testing and verification

Logic Synthesis for Asynchronous Controllers and Interfaces J. Cortadella, M. Kishinevsky, A. Kondratyev, Luciano Lavagno, Alex Yakovlev, 2012-12-06 This book is the result of a long friendship of a broad international co operation and of a bold dream It is the summary of work carried out by the authors and several other wonderful people during more than 15 years across 3 continents in the course of countless meetings workshops and discussions It shows that neither language nor distance can be an obstacle to close scientific cooperation when there is unity of goals and true collaboration When we started we had very different approaches to handling the mysterious almost magical world of asynchronous circuits Some

were more theoretical some were closer to physical reality some were driven mostly by design needs In the end we all shared the same belief that true Electronic Design Automation research must be solidly grounded in formal models practically minded to avoid excessive complexity and tested in the field in the form of experimental tools The results are this book and the CAD tool petrify The latter can be downloaded and tried by anybody bold or desperate enough to tread into the clockless but not lawless domain of small scale asynchronicity The URL is <http://www.lsi.upc.es/jordic/petrify> We believe that asynchronous circuits are a wonderful object that abandons some of the almost militaristic law and order that governs synchronous circuits to improve in terms of simplicity energy efficiency and performance

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