

LOGICALLY DETERMINED DESIGN

*Clockless System Design with NULL
Convention Logic™*



KARL M. FANT

Logically Determined Design Clockless System Design With Null Convention Logic

Arthur D. Friedman



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Logically Determined Design Karl M. Fant, 2005-02-22 This seminal book presents a new logically determined design methodology for designing clockless circuit systems The book presents the foundations architectures and methodologies to implement such systems Based on logical relationships it concentrates on digital circuit system complexity and productivity to allow for more reliable faster and cheaper products Transcends shortcomings of Boolean logic Presents theoretical foundations architecture and analysis of clockless asynchronous circuit design Contains examples and exercises making it ideal for those studying the area

Computer Science Reconsidered Karl M. Fant, 2007-06-04 The Invocation Model of Process Expression argues that mathematics does not provide the most appropriate conceptual foundations for computer science but rather that these foundations are a primary source of unnecessary complexity and confusion It supports that there is a more appropriate conceptual model that unifies forms of expression considered quite disparate and simplifies issues considered complex and intractable This book presents that this model of process expression is alternative theory of computer science that is both valid and practical

VLSI-SoC: From Algorithms to Circuits and System-on-Chip Design Andreas Burg, Ayse Coskun, Matthew Guthaus, Srinivas Katkoori, Ricardo Reis, 2013-11-26 This book contains extended and revised versions of the best papers presented at the 20th IFIP WG 10.5 IEEE International Conference on Very Large Scale Integration VLSI SoC 2012 held in Santa Cruz CA USA in October 2012 The 12 papers included in the book were carefully reviewed and selected from the 33 full papers presented at the conference The papers cover a wide range of topics in VLSI technology and advanced research They address the current trend toward increasing chip integration and technology process advancements bringing about stimulating new challenges both at the physical and system design levels as well as in the test of these systems

Innovations in Electronics and Communication Engineering H. S. Saini, R. K. Singh, K. Satish Reddy, 2017-11-08 The book contains high quality papers presented in the Fifth International Conference on Innovations in Electronics and Communication Engineering ICIECE 2016 held at Guru Nanak Institutions Hyderabad India during 8 and 9 July 2016 The objective is to provide the latest developments in the field of electronics and communication engineering specially the areas like Image Processing Wireless Communications Radar Signal Processing Embedded Systems and VLSI Design The book aims to provide an opportunity for researchers scientists technocrats academicians and engineers to exchange their innovative ideas and research findings in the field of Electronics and Communication Engineering

Design Automation of Real-Life Asynchronous Devices and Systems Alexander Taubin, Jordi Cortadella, Luciano Lavagno, 2007 The number of gates on a chip is quickly growing toward and beyond the one billion mark Keeping all the gates running at the beat of a single or a few rationally related clocks is becoming impossible In static timing analysis process variations and signal integrity issues stretch the timing margins to the point where they become too conservative and result in significant overdesign Importance and difficulty of such problems push some developers to once again turn to

asynchronous alternatives However the electronics industry for the most part is still reluctant to adopt asynchronous design with a few notable exceptions due to a common belief that we still lack a commercial quality Electronic Design Automation tools similar to the synchronous RTL to GDSII flow for asynchronous circuits The purpose of this paper is to counteract this view by presenting design flows that can tackle large designs without significant changes with respect to synchronous design flow We are limiting ourselves to four design flows that we believe to be closest to this goal We start from the Tangram flow because it is the most commercially proven and it is one of the oldest from a methodological point of view The other three flows Null Convention Logic de synchronization and gate level pipelining could be considered together as asynchronous re implementations of synchronous RTL or gate level specifications The main common idea is substituting the global clocks by local synchronizations Their most important aspect is to open the possibility to implement large legacy synchronous designs in an almost push button manner where all asynchronous machinery is hidden so that synchronous RTL designers do not need to be re educated These three flows offer a trade off from very low overhead almost synchronous implementations to very high performance extremely robust dual rail pipelines

IAENG Transactions on Engineering Technologies Sio-Iong Ao,2012 This volume contains revised and extended research articles by prominent researchers Topics covered include operations research scientific computing industrial engineering electrical engineering communication systems and industrial applications The book offers the state of the art advances in engineering technologies and also serves as an excellent reference work for researchers and graduate students working with on engineering technologies

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Wireless Interface Technologies for 3D IC and Module Integration Tadahiro Kuroda,Wai-Yeung Yip,2021-09-30 Synthesising fifteen years of research this authoritative text provides a comprehensive treatment of two major technologies for wireless chip and module interface design covering technology fundamentals design considerations and tradeoffs practical implementation considerations and discussion of practical applications in neural network reconfigurable processors and stacked SRAM It explains the design principles and applications of two near field wireless interface technologies for 2 5 3D IC and module integration respectively and describes system level performance benefits making this an essential resource for researchers professional engineers and graduate students performing research in next generation wireless chip and module interface design

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