

Why Test? Why Add Test Logic?

■ Why test?

- Measurement of defects & quality level
- Incoming inspection contractual
- Perceived product quality by customer
- Reliability requirement contractual

■ Why add test logic?

- To increase the test coverage
- To reduce the time it takes to quality the part
- To reduce the cost-of-test

■ Design For Testability

- The act of adding logic or features to enhance the testability of a design is generally referred to as Design-for-Test (DFT)

Logic Testing And Design For Testability

J. Altet, Antonio Rubio



Logic Testing And Design For Testability:

Logic Testing and Design for Testability Hideo Fujiwara, 1985-06 Design for testability techniques offer one approach toward alleviating this situation by adding enough extra circuitry to a circuit or chip to reduce the complexity of testing Today's computers must perform with increasing reliability which in turn depends on the problem of determining whether a circuit has been manufactured properly or behaves correctly However the greater circuit density of VLSI circuits and systems has made testing more difficult and costly This book notes that one solution is to develop faster and more efficient algorithms to generate test patterns or use design techniques to enhance testability that is design for testability Design for testability techniques offer one approach toward alleviating this situation by adding enough extra circuitry to a circuit or chip to reduce the complexity of testing Because the cost of hardware is decreasing as the cost of testing rises there is now a growing interest in these techniques for VLSI circuits The first half of the book focuses on the problem of testing test generation fault simulation and complexity of testing The second half takes up the problem of design for testability design techniques to minimize test application and or test generation cost scan design for sequential logic circuits compact testing built in testing and various design techniques for testable systems **Logic Testing and Design for Testability** is included in the Computer Systems Series edited by Herb Schwetman

On-Line Testing for VLSI Michael Nicolaidis, Yervant Zorian, Dhiraj Pradhan, 2013-03-09 Test functions fault detection diagnosis error correction repair etc that are applied concurrently while the system continues its intended function are defined as on line testing In its expanded scope on line testing includes the design of concurrent error checking subsystems that can be themselves self checking fail safe systems that continue to function correctly even after an error occurs reliability monitoring and self test and fault tolerant designs **On Line Testing for VLSI** contains a selected set of articles that discuss many of the modern aspects of on line testing as faced today The contributions are largely derived from recent IEEE International On Line Testing Workshops Guest editors Michael Nicolaidis Yervant Zorian and Dhiraj Pradhan organized the articles into six chapters In the first chapter the editors introduce a large number of approaches with an expanded bibliography in which some references date back to the sixties **On Line Testing for VLSI** is an edited volume of original research comprising invited contributions by leading researchers

VLSI Test Principles and Architectures Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen, 2006-08-14 This book is a comprehensive guide to new DFT methods that will show the readers how to design a testable and quality product drive down test cost improve product quality and yield and speed up time to market and time to volume Most up to date coverage of design for testability Coverage of industry practices commonly found in commercial DFT tools but not discussed in other books Numerous practical examples in each chapter illustrating basic VLSI test principles and DFT architectures **Logic Testing and Design for Testability** E. N. Murphy, Electrical Engineering and Electronics, 1985 **Digital Circuit Testing and Testability** Parag K. Lala, 1997 An easy to use introduction to the practices and techniques in the field of digital circuit

testing Lala writes in a user friendly and tutorial style making the book easy to read even for the newcomer to fault tolerant system design Each informative chapter is self contained with little or no previous knowledge of a topic assumed Extensive references follow each chapter *Testability Concepts for Digital ICs* F.P.M. Beenker,R.G. Bennetts,A.P.

Thijssen,2012-12-06 Preface Testing Integrated Circuits for manufacturing defects includes four basic disciplines First of all an understanding of the origin and behaviour of defects Secondly knowledge of IC design and IC design styles Thirdly knowledge of how to create a test program for an IC which is targeted on detecting these defects and finally understanding of the hardware Automatic Test Equipment to run the test on All four items have to be treated managed and to a great extent integrated before the term IC quality gets a certain meaning and a test a certain measurable value The contents of this book reflects our activities on testability concepts for complex digital ICs as performed at Philips Research Laboratories in Eindhoven The Netherlands Based on the statements above we have worked along a long term plan which was based on four pillars 1 The definition of a test methodology suitable for future IC design styles 2 capable of handling improved defect models 3 supported by software tools and 4 providing an easy link to Automatic Test Equipment The reasoning we have followed was continuously focused on IC qUality Quality expressed in terms of the ability of delivering a customer a device with no residual manufacturing defects Bad devices should not escape a test The basis of IC quality is a thorough understanding of defects and defect models *Principles of Testing Electronic Systems* Samiha Mourad,Yervant Zorian,2000-07-25 A pragmatic approach to testing electronic systems As we move ahead in the electronic age rapid changes in technology pose an ever increasing number of challenges in testing electronic products Many practicing engineers are involved in this arena but few have a chance to study the field in a systematic way learning takes place on the job By covering the fundamental disciplines in detail Principles of Testing Electronic Systems provides design engineers with the much needed knowledge base Divided into five major parts this highly useful reference relates design and tests to the development of reliable electronic products shows the main vehicles for design verification examines designs that facilitate testing and investigates how testing is applied to random logic memories FPGAs and microprocessors Finally the last part offers coverage of advanced test solutions for today s very deep submicron designs The authors take a phenomenological approach to the subject matter while providing readers with plenty of opportunities to explore the foundation in detail Special features include An explanation of where a test belongs in the design flow Detailed discussion of scan path and ordering of scan chains BIST solutions for embedded logic and memory blocks Test methodologies for FPGAs A chapter on testing system on a chip Numerous references **Designer's Guide to Testable Asic Devices** Wayne M. Needham,1991-01-10 While making up a larger percentage of the total number of designs produced each year ASICs present special problems for system designers in the area of testing because each design is complex and unique This book shows readers how to apply basic test techniques to ASIC design details the impact of ASIC testability on total system cost and performance and reviews the

commercial test systems that are currently available Annotation copyrighted by Book News Inc Portland OR

Thermal Testing of Integrated Circuits J. Altet, Antonio Rubio, 2013-03-09 Integrated circuits IC s have undergone a significant evolution in terms of complexity and performance as a result of the substantial advances made in manufacturing technology Circuits in their various mixed formats can be made up tens or even hundreds of millions of devices They work at extremely low voltages and switch at very high frequencies Testing of circuits has become an essential process in IC manufacturing in the effort to ensure that the manufactured components have the appropriate levels of quality Along with the ongoing trend towards more advanced technology and circuit features major testing challenges are continuously emerging The use of ambivalent procedures to test the analogue and digital sections of such complex circuits without interfering in their nominal operation is clearly a critical part of today s technological ipdustries Chapter 1 presents the general purposes and basic concepts rel ted With thetesting of integrated circuits discussing the various strategies and their limitations Readers who are already familiar with the field may opt to skip this chapter This book offers a multidisciplinary focus on thermal testing This is a testing method which is not only suitable for use in combination with other existing techniques but is also backed by a wealth of knowledge and offers exciting opportunities in the form of as yet unexplored areas of research and innovation for industrial applications

Protocol Test Systems VIII Ana Cavalli, Stan Budkowski, 2013-03-09 IWPTS 95 International Workshop on Protocol Test Systems is being held this year at NT Institut National des Telecommunications Evry France from 4 to 6 September 1995 IWPTS 95 is the eighth of a series of annual meetings sponsored by the IFIP Working Group WG6 1 dedicated to Architecture and Protocols for Computer Networks The seven previous workshops were held in Vancouver Canada 1988 Berlin Germany 1989 Mclean USA 1990 Leidschendam The Netherlands 1991 Montreal Canada 1992 Pau France 1993 and Tokyo Japan 1994 The workshop is a meeting place where both research and industry theory and practice come together By bringing both researchers and practitioners together IWPTS opens up the communication between these groups This helps keep the research vital and improves the state of the practitioner s art Forty eight papers have been submitted to IWPTS 95 and all of them have been reviewed by the members of the Program Committee and additional reviewers The completed reviewers list is included in this Proceedings Based on these reviews the Program Committee selected 26 for oral presentation and 4 to be presented as posters Two specially invited papers complete the Workshop Program which is composed of ten sessions Testing Methods Session 1 Test Environments Session 2 Theoretical Framework Session 3 Algorithms and Languages Session 4 Test Generation 1 Session 5 Testability Session 6 Test Generation 2 Session 7 Industrial Applications Session 8 Distributed Testing and performance Session 9 and Test Management Session 10

VLSI Testing Stanley Leonard Hurst, 1998 Hurst an editor at the Microelectronics Journal analyzes common problems that electronics engineers and circuit designers encounter while testing integrated circuits and the systems in which they are used and explains a variety of solutions available for overcoming them in both digital and mixed circuits Among his topics are

faults in digital circuits generating a digital test pattern signatures and self tests structured design for testability testing structured digital circuits and microprocessors and financial aspects of testing The self contained reference is also suitable as a textbook in a formal course on the subject Annotation copyrighted by Book News Inc Portland OR **Testing and Diagnosis of VLSI and ULSI** F. Lombardi, M.G. Sami, 2012-12-06 This volume contains a collection of papers presented at the NATO Advanced Study Institute on Testing and Diagnosis of VLSI and ULSI held at Villa Olmo Como Italy June 22 July 3 1987 High Density technologies such as Very Large Scale Integration VLSI Wafer Scale Integration WSI and the not so far promises of Ultra Large Scale Integration ULSI have exasperated the problema associated with the testing and diagnosis of these devices and systema Traditional techniques are fast becoming obsolete due to unique requirements such as limited controllability and observability increasing execution complexity for test vector generation and high cost of fault simulation to mention just a few New approaches are imperative to achieve the highly sought goal of the three months turn around cycle time for a state of the art computer chip The importance of testing and diagnostic processes is of primary importance if costs must be kept at acceptable levels The objective of this NATO ASI was to present analyze and discuss the various facets of testing and diagnosis with respect to both theory and practice The contents of this volume reflect the diversity of approaches currently available to reduce test and diagnosis time These approaches are described in a concise yet clear way by renowned experts of the field Their contributions are aimed at a wide readership the uninitiated researcher will find the tutorial chapters very rewarding The expert will be introduced to advanced techniques in a very comprehensive manner *Digital Logic Testing and Simulation* Alexander Miczo, 2003-10-24 Your road map for meeting today s digital testing challenges Today digital logic devices are common in products that impact public safety including applications in transportation and human implants Accurate testing has become more critical to reliability safety and the bottom line Yet as digital systems become more ubiquitous and complex the challenge of testing them has become more difficult As one development group designing a RISC stated the work required to test a chip of this size approached the amount of effort required to design it A valued reference for nearly two decades Digital Logic Testing and Simulation has been significantly revised and updated for designers and test engineers who must meet this challenge There is no single solution to the testing problem Organized in an easy to follow sequential format this Second Edition familiarizes the reader with the many different strategies for testing and their applications and assesses the strengths and weaknesses of the various approaches The book reviews the building blocks of a successful testing strategy and guides the reader on choosing the best solution for a particular application Digital Logic Testing and Simulation Second Edition covers such key topics as Binary Decision Diagrams BDDs and cycle based simulation Tester architectures Standard Test Interface Language STIL Practical algorithms written in a Hardware Design Language HDL Fault tolerance Behavioral Automatic Test Pattern Generation ATPG The development of the Test Design Expert TDX the many obstacles encountered and lessons learned in creating this novel testing approach Up to date and comprehensive

Digital Logic Testing and Simulation is an important resource for anyone charged with pinpointing faulty products and assuring quality safety and profitability

SOC (System-on-a-Chip) Testing for Plug and Play Test Automation Krishnendu Chakrabarty, 2013-04-17 System on a Chip SOC integrated circuits composed of embedded cores are now commonplace Nevertheless there remain several roadblocks to rapid and efficient system integration Test development is seen as a major bottleneck in SOC design and manufacturing capabilities Testing SOC is especially challenging in the absence of standardized test structures test automation tools and test protocols In addition long interconnects high density and high speed designs lead to new types of faults involving crosstalk and signal integrity SOC System on a Chip Testing for Plug and Play Test Automation is an edited work containing thirteen contributions that address various aspects of SOC testing SOC System on a Chip Testing for Plug and Play Test Automation is a valuable reference for researchers and students interested in various aspects of SOC testing

Digital System Test and Testable Design Zainalabedin Navabi, 2010-12-10 This book is about digital system testing and testable design The concepts of testing and testability are treated together with digital design practices and methodologies The book uses Verilog models and testbenches for implementing and explaining fault simulation and test generation algorithms Extensive use of Verilog and Verilog PLI for test applications is what distinguishes this book from other test and testability books Verilog eliminates ambiguities in test algorithms and BIST and DFT hardware architectures and it clearly describes the architecture of the testability hardware and its test sessions Describing many of the on chip decompression algorithms in Verilog helps to evaluate these algorithms in terms of hardware overhead and timing and thus feasibility of using them for System on Chip designs Extensive use of testbenches and testbench development techniques is another unique feature of this book Using PLI in developing testbenches and virtual testers provides a powerful programming tool interfaced with hardware described in Verilog This mixed hardware software environment facilitates description of complex test programs and test strategies

A Practical Approach to VLSI System on Chip (SoC) Design Veena S. Chakravarthi, 2022-12-13 Now in a thoroughly revised second edition this practical practitioner guide provides a comprehensive overview of the SoC design process It explains end to end system on chip SoC design processes and includes updated coverage of design methodology the design environment EDA tool flow design decisions choice of design intellectual property IP cores sign off procedures and design infrastructure requirements The second edition provides new information on SOC trends and updated design cases Coverage also includes critical advanced guidance on the latest UPF based low power design flow challenges of deep submicron technologies and 3D design fundamentals which will prepare the readers for the challenges of working at the nanotechnology scale A Practical Approach to VLSI System on Chip SoC Design A Comprehensive Guide Second Edition provides engineers who aspire to become VLSI designers with all the necessary information and details of EDA tools It will be a valuable professional reference for those working on VLSI design and verification portfolios in complex SoC designs

Wafer Scale Integration Earl E. Swartzlander Jr., 2012-12-06 Wafer

Scale Integration WSI is the culmination of the quest for larger integrated circuits In VLSI chips are developed by fabricating a wafer with hundreds of identical circuits testing the circuits dicing the wafer and packaging the good dice In contrast in WSI a wafer is fabricated with several types of circuits generally referred to as cells with multiple instances of each cell type the cells are tested and good cells are interconnected to realize a system on the wafer Since most signal lines stay on the wafer stray capacitance is low so that high speeds are achieved with low power consumption For the same technology a WSI implementation may be a factor of five faster dissipate a factor of ten less power and require one hundredth to one thousandth the volume Successful development of WSI involves many overlapping disciplines ranging from architecture to test design to fabrication including laser linking and cutting multiple levels of interconnection and packaging This book concentrates on the areas that are unique to WSI and that are as a result not well covered by any of the many books on VLSI design A unique aspect of WSI is that the finished circuits are so large that there will be defects in some portions of the circuit Accordingly much attention must be devoted to designing architectures that facilitate fault detection and reconfiguration to of WSI include fabrication circumvent the faults Other unique aspects technology and packaging

Design of VLSI Circuits Egon Hörbst, Christian Müller-Schloer, Heinz Schwärtzel, 2012-12-06 Microelectronics are certainly one of the key technologies of our time They are a key factor of technological and economic progress They effect the fields of automation information and communication leading to the development of new applications and markets Attention should be focused on three areas of development process and production technology test technology design technology Clearly because of the development of new application fields the skill of design ing integrated circuits should not be limited to a few highly specialized experts Rather this ability should be made available to all system and design engineers as a new application technology just like programming technology for software For this reason design procedures have to be developed which supported by appropriate CAD systems provide the designer with tools for representation of effective instruments for design and reliable tools for verification ensuring simple proper and easily controllable interfaces for the manufacturing and test processes Such CAD systems are called standard design systems They open the way to fast and safe design of integrated circuits First this book demonstrates basic principles with an example of the Siemens design system VENUS gives a general introduction to the method of designing integrated circuits familiarizes the reader with basic semiconductor and circuit technologies shows the various methods of layout design and presents necessary concepts and strategies of test technology

Computer-Aided Verification Edmund M. Clarke, Robert P. Kurshan, 1991-10-02 This volume contains the proceedings of the second workshop on Computer Aided Verification held at DIMACS Rutgers University June 18-21 1990 It features theoretical results that lead to new or more powerful verification methods Among these are advances in the use of binary decision diagrams dense time reductions based upon partial order representations and proof checking in controller verification The motivation for holding a workshop on computer aided verification was to bring together work on

effective algorithms or methodologies for formal verification as distinguished say from attributes of logics or formal languages The considerable interest generated by the first workshop held in Grenoble June 1989 see LNCS 407 prompted this second meeting The general focus of this volume is on the problem of making formal verification feasible for various models of computation Specific emphasis is on models associated with distributed programs protocols and digital circuits The general test of algorithm feasibility is to embed it into a verification tool and exercise that tool on realistic examples the workshop included sessions for the demonstration of new verification tools

Design for AT-Speed Test, Diagnosis and Measurement Benoit Nadeau-Dostie, 2006-04-11 Design for AT Speed Test Diagnosis and Measurement is the first book to offer practical and proven design for testability DFT solutions to chip and system design engineers test engineers and product managers at the silicon level as well as at the board and systems levels Designers will see how the implementation of embedded test enables simplification of silicon debug and system bring up Test engineers will determine how embedded test provides a superior level of at speed test diagnosis and measurement without exceeding the capabilities of their equipment Product managers will learn how the time resources and costs associated with test development manufacture cost and lifecycle maintenance of their products can be significantly reduced by designing embedded test in the product A complete design flow and analysis of the impact of embedded test on a design makes this book a must read before any DFT is attempted

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Logic Testing And Design For Testability Introduction

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obstacles and a plan for the future pros allows managers and human to recalibrate before the year is over

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