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# Embedded Processorbased Selftest

**Dimitris Gizopoulos**



## **Embedded Processorbased Selftest:**

**Embedded Processor-Based Self-Test** Dimitris Gizopoulos,A. Paschalis,Yervant Zorian,2004-12-20 Embedded Processor Based Self Test is a guide to self testing strategies for embedded processors Embedded processors are regularly used today in most System on Chips SoCs Testing of microprocessors and embedded processors has always been a challenge because most traditional testing techniques fail when applied to them This is due to the complex sequential structure of processor architectures which consists of high performance datapath units and sophisticated control logic for performance optimization Structured Design for Testability DfT and hardware based self testing techniques which usually have a non trivial impact on a circuit s performance size and power can not be applied without serious consideration and careful incorporation into the processor design Embedded Processor Based Self Test shows how the powerful embedded functionality that processors offer can be utilized as a self testing resource Through a discussion of different strategies the book emphasizes on the emerging area of Software Based Self Testing SBST SBST is based on the idea of execution of embedded software programs to perform self testing of the processor itself and its surrounding blocks in the SoC SBST is a low cost strategy in terms of overhead area speed power development effort and test application cost as it is applied using low cost low speed test equipment Embedded Processor Based Self Test can be used by designers DfT engineers test practitioners researchers and students working on digital testing and in particular processor and SoC test This book sets the framework for comparisons among different SBST methodologies by discussing key requirements It presents successful applications of SBST to a number of embedded processors of different complexities and instruction set architectures

*Embedded Processor-Based Self-Test* Dimitris Gizopoulos,A. Paschalis,Yervant Zorian,2013-03-09 Embedded Processor Based Self Test is a guide to self testing strategies for embedded processors Embedded processors are regularly used today in most System on Chips SoCs Testing of microprocessors and embedded processors has always been a challenge because most traditional testing techniques fail when applied to them This is due to the complex sequential structure of processor architectures which consists of high performance datapath units and sophisticated control logic for performance optimization Structured Design for Testability DfT and hardware based self testing techniques which usually have a non trivial impact on a circuit s performance size and power can not be applied without serious consideration and careful incorporation into the processor design Embedded Processor Based Self Test shows how the powerful embedded functionality that processors offer can be utilized as a self testing resource Through a discussion of different strategies the book emphasizes on the emerging area of Software Based Self Testing SBST SBST is based on the idea of execution of embedded software programs to perform self testing of the processor itself and its surrounding blocks in the SoC SBST is a low cost strategy in terms of overhead area speed power development effort and test application cost as it is applied using low cost low speed test equipment Embedded Processor Based Self Test can be used by designers DfT engineers test practitioners researchers and students working on

digital testing and in particular processor and SoC test This book sets the framework for comparisons among different SBST methodologies by discussing key requirements It presents successful applications of SBST to a number of embedded processors of different complexities and instruction set architectures Embedded Processor-Based Self-Test Gizopoulos,2009-05-01

**Processor Design** Jari Nurmi,2007-07-26 Processor Design provides insight into a number of different flavors of processor architectures and their design software tool generation implementation and verification After a brief introduction to processor architectures and how processor designers have sometimes failed to deliver what was expected the authors introduce a generic flow for embedded on chip processor design and start to explore the vast design space of on chip processing The types of processor cores covered include general purpose RISC cores traditional DSP a VLIW approach to signal processing processor cores that can be customized for specific applications reconfigurable processors protocol processors Java engines and stream processors Co processor and multi core design approaches that deliver application specific performance over and above that which is available from single core designs are also described

**SOC (System-on-a-Chip) Testing for Plug and Play Test Automation** Krishnendu Chakrabarty,2013-04-17 System on a Chip SOC integrated circuits composed of embedded cores are now commonplace Nevertheless there remain several roadblocks to rapid and efficient system integration Test development is seen as a major bottleneck in SOC design and manufacturing capabilities Testing SOC is especially challenging in the absence of standardized test structures test automation tools and test protocols In addition long interconnects high density and high speed designs lead to new types of faults involving crosstalk and signal integrity

**SOC System on a Chip Testing for Plug and Play Test Automation** is an edited work containing thirteen contributions that address various aspects of SOC testing SOC System on a Chip Testing for Plug and Play Test Automation is a valuable reference for researchers and students interested in various aspects of SOC testing

*Railway Safety, Reliability, and Security: Technologies and Systems Engineering* Flammini, Francesco,2012-05-31 Human errors as well as deliberate sabotage pose a considerable danger to passengers riding on the modern railways and have created disastrous consequences To protect civilians against both intentional and unintentional threats rail transportation has become increasingly automated

**Railway Safety Reliability and Security Technologies and Systems Engineering** provides engineering students and professionals with a collection of state of the art methodological and technological notions to support the development and certification of real time safety critical railway control systems as well as the protection of rail transportation infrastructures

**Software-based Self-test and Diagnosis for Processors and System-on-chips** Li Chen,2003

**Advanced Industrial Control Technology** Peng Zhang,2010-08-26 Control engineering seeks to understand physical systems using mathematical modeling in terms of inputs outputs and various components with different behaviors It has an essential role in a wide range of control systems from household appliances to space flight This book provides an in depth view of the technologies that are implemented in most varieties of modern industrial control engineering A solid

grounding is provided in traditional control techniques followed by detailed examination of modern control techniques such as real time distributed robotic embedded computer and wireless control technologies For each technology the book discusses its full profile from the field layer and the control layer to the operator layer It also includes all the interfaces in industrial control systems between controllers and systems between different layers and between operators and systems It not only describes the details of both real time operating systems and distributed operating systems but also provides coverage of the microprocessor boot code which other books lack In addition to working principles and operation mechanisms this book emphasizes the practical issues of components devices and hardware circuits giving the specification parameters install procedures calibration and configuration methodologies needed for engineers to put the theory into practice Documents all the key technologies of a wide range of industrial control systems Emphasizes practical application and methods alongside theory and principles An ideal reference for practicing engineers needing to further their understanding of the latest industrial control concepts and techniques

### **System-on-Chip Test Architectures**

Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, 2010-07-28 Modern electronics testing has a legacy of more than 40 years The introduction of new technologies especially nanometer technologies with 90nm or smaller geometry has allowed the semiconductor industry to keep pace with the increased performance capacity demands from consumers As a result semiconductor test costs have been growing steadily and typically amount to 40% of today's overall product cost This book is a comprehensive guide to new VLSI Testing and Design for Testability techniques that will allow students researchers DFT practitioners and VLSI designers to master quickly System on Chip Test architectures for test debug and diagnosis of digital memory and analog mixed signal designs Emphasizes VLSI Test principles and Design for Testability architectures with numerous illustrations examples Most up to date coverage available including Fault Tolerance Low Power Testing Defect and Error Tolerance Network on Chip NOC Testing Software Based Self Testing FPGA Testing MEMS Testing and System In Package SIP Testing which are not yet available in any testing book Covers the entire spectrum of VLSI testing and DFT architectures from digital and analog to memory circuits and fault diagnosis and self repair from digital to memory circuits Discusses future nanotechnology test trends and challenges facing the nanometer design era promising nanotechnology test techniques including Quantum Dots Cellular Automata Carbon Nanotubes and Hybrid Semiconductor Nanowire Molecular Computing Practical problems at the end of each chapter for students

### **Design and Test Technology for Dependable**

**Systems-on-Chip** Ubar, Raimund, Raik, Jaan, Vierhaus, Heinrich Theodor, 2010-12-31 This book covers aspects of system design and efficient modelling and also introduces various fault models and fault mechanisms associated with digital circuits integrated into System on Chip SoC Multi Processor System on Chip MPSoC or Network on Chip NoC

**VLSI-SoC: New Technology Enabler** Carolina Metzler, Pierre-Emmanuel Gaillardon, Giovanni De Micheli, Carlos Silva-Cardenas, Ricardo Reis, 2020-07-22 This book contains extended and revised versions of the best papers presented at the 27th IFIP WG 10.5

IEEE International Conference on Very Large Scale Integration VLSI SoC 2019 held in Cusco Peru in October 2019 The 15 full papers included in this volume were carefully reviewed and selected from the 28 papers out of 82 submissions presented at the conference The papers discuss the latest academic and industrial results and developments as well as future trends in the field of System on Chip SoC design considering the challenges of nano scale state of the art and emerging manufacturing technologies In particular they address cutting edge research fields like heterogeneous neuromorphic and brain inspired biologically inspired approximate computing systems

**Embedded Systems Handbook** Richard Zurawski, 2005-08-16

Embedded systems are nearly ubiquitous and books on individual topics or components of embedded systems are equally abundant Unfortunately for those designers who thirst for knowledge of the big picture of embedded systems there is not a drop to drink Until now The Embedded Systems Handbook is an oasis of information offering a mix of basic a

*System-level Test and Validation of Hardware/Software Systems* Zebo Peng, 2005-04-07 New manufacturing technologies have made possible the integration of entire systems on a single chip This new design paradigm termed system on chip SOC together with its associated manufacturing problems represents a real challenge for designers SOC is also reshaping approaches to test and validation activities These are beginning to migrate from the traditional register transfer or gate levels of abstraction to the system level Until now test and validation have not been supported by system level design tools so designers have lacked the infrastructure to exploit all the benefits stemming from the adoption of the system level of abstraction Research efforts are already addressing this issue This monograph provides a state of the art overview of the current validation and test techniques by covering all aspects of the subject including modeling of bugs and defects stimulus generation for validation and test purposes including timing errors design for testability

**The Dark Side of Silicon** Amir M. Rahmani, Pasi Liljeberg, Ahmed Hemani, Axel Jantsch, Hannu Tenhunen, 2016-12-31 This book presents the state of the art of one of the main concerns with microprocessors today a phenomenon known as dark silicon Readers will learn how power constraints both leakage and dynamic power limit the extent to which large portions of a chip can be powered up at a given time i e how much actual performance and functionality the microprocessor can provide The authors describe their research toward the future of microprocessor development in the dark silicon era covering a variety of important aspects of dark silicon aware architectures including design management reliability and test Readers will benefit from specific recommendations for mitigating the dark silicon phenomenon including energy efficient dedicated solutions and technologies to maximize the utilization and reliability of microprocessors

Processor Description Languages Prabhat Mishra, Nikil Dutt, 2011-07-28 Efficient design of embedded processors plays a critical role in embedded systems design Processor description languages and their associated specification exploration and rapid prototyping methodologies are used to find the best possible design for a given set of applications under various design constraints such as area power and performance This book is the first comprehensive survey of modern architecture description languages and will be an invaluable reference

for embedded system architects designers developers and validation engineers Readers will see that the use of particular architecture description languages will lead to productivity gains in designing particular application specific types of embedded processors Comprehensive coverage of all modern architecture description languages use the right ADL to design your processor to fit your application Most up to date information available about each architecture description language from the developers save time chasing down reliable documentation Describes how each architecture description language enables key design automation tasks such as simulation synthesis and testing fit the ADL to your design cycle VLSI-SoC:

At the Crossroads of Emerging Trends Alex Orailoglu,H. Fatih Ugurdag,Luís Miguel Silveira,Martin Margala,Ricardo Reis,2015-09-25 This book contains extended and revised versions of the best papers presented at the 21st IFIP WG 10 5 IEEE International Conference on Very Large Scale Integration VLSI SoC 2013 held in Istanbul Turkey in October 2013 The 11 papers included in the book were carefully reviewed and selected from the 48 full papers presented at the conference An extended version of a previously unpublished high quality paper from VLSI SoC 2012 is also included The papers cover a wide range of topics in VLSI technology and advanced research They address the current trend toward increasing chip integration and technology process advancements bringing about stimulating new challenges both at the physical and system design levels as well as in the test of these systems **Advances in Electronic Testing** Dimitris Gizopoulos,2006-01-22

This is a new type of edited volume in the Frontiers in Electronic Testing book series devoted to recent advances in electronic circuits testing The book is a comprehensive elaboration on important topics which capture major research and development efforts today Hot topics of current interest to test technology community have been selected and the authors are key contributors in the corresponding topics **Oscillation-Based Test in Mixed-Signal Circuits** Gloria Huertas

Sánchez,Diego Vázquez García de la Vega,Adoración Rueda Rueda,Jose Luis Huertas Díaz,2007-06-03 This book presents the development and experimental validation of the structural test strategy called Oscillation Based Test OBT in short The results presented here assert not only from a theoretical point of view but also based on a wide experimental support that OBT is an efficient defect oriented test solution complementing the existing functional test techniques for mixed signal circuits

*VLSI-SoC: From Algorithms to Circuits and System-on-Chip Design* Andreas Burg,Ayşe Coskun,Matthew Guthaus,Srinivas Katkoori,Ricardo Reis,2013-11-26 This book contains extended and revised versions of the best papers presented at the 20th IFIP WG 10 5 IEEE International Conference on Very Large Scale Integration VLSI SoC 2012 held in Santa Cruz CA USA in October 2012 The 12 papers included in the book were carefully reviewed and selected from the 33 full papers presented at the conference The papers cover a wide range of topics in VLSI technology and advanced research They address the current trend toward increasing chip integration and technology process advancements bringing about stimulating new challenges both at the physical and system design levels as well as in the test of these systems **Fault-Tolerance Techniques for**

**SRAM-Based FPGAs** Fernanda Lima Kastensmidt,Ricardo Reis,2007-02-01 Fault tolerance in integrated circuits is not an

exclusive concern regarding space designers or highly reliable application engineers. Rather, designers of next generation products must cope with reduced margin noises due to technological advances. The continuous evolution of the fabrication technology process of semiconductor components in terms of transistor geometry shrinking, power supply speed and logic density has significantly reduced the reliability of very deep submicron integrated circuits in face of the various internal and external sources of noise. The very popular Field Programmable Gate Arrays (FPGAs) customizable by SRAM cells are a consequence of the integrated circuit evolution with millions of memory cells to implement the logic embedded memories, routing and more recently with embedded microprocessors cores. These re-programmable systems on chip platforms must be fault tolerant to cope with present day requirements. This book discusses fault tolerance techniques for SRAM based Field Programmable Gate Arrays (FPGAs). It starts by showing the model of the problem and the upset effects in the programmable architecture. In the sequence, it shows the main fault tolerance techniques used nowadays to protect integrated circuits against errors. A large set of methods for designing fault tolerance systems in SRAM based FPGAs is described. Some presented techniques are based on developing a new fault tolerant architecture with new robustness FPGA elements. Other techniques are based on protecting the high level hardware description before the synthesis in the FPGA. The reader has the flexibility of choosing the most suitable fault tolerance technique for its project and to compare a set of fault tolerant techniques for programmable logic applications.



## Reviewing **Embedded Processorbased Selftest**: Unlocking the Spellbinding Force of Linguistics

In a fast-paced world fueled by information and interconnectivity, the spellbinding force of linguistics has acquired newfound prominence. Its capacity to evoke emotions, stimulate contemplation, and stimulate metamorphosis is truly astonishing. Within the pages of "**Embedded Processorbased Selftest**," an enthralling opus penned by a very acclaimed wordsmith, readers attempt an immersive expedition to unravel the intricate significance of language and its indelible imprint on our lives. Throughout this assessment, we shall delve to the book is central motifs, appraise its distinctive narrative style, and gauge its overarching influence on the minds of its readers.

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### Embedded Processorbased Selftest Introduction

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