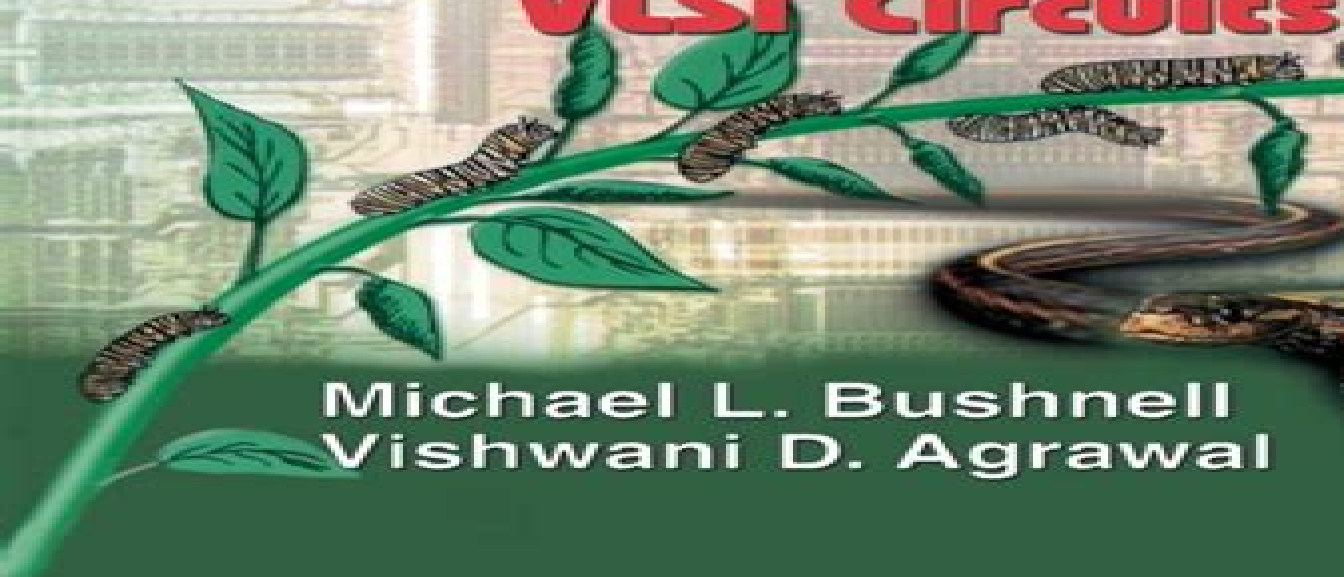


# Essentials of Electronic Testing



**for Digital,  
Memory &  
Mixed-Signal  
VLSI Circuits**



Michael L. Bushnell  
Vishwani D. Agrawal

# Essentials Of Electronic Testing For Digital Memory And Mixed Signal Vlsi Circuits

**R. Dean Adams**



## **Essentials Of Electronic Testing For Digital Memory And Mixed Signal Vlsi Circuits:**

**Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits** M. Bushnell, Vishwani Agrawal, 2006-04-11 The modern electronic testing has a forty year history Test professionals hold some fairly large conferences and numerous workshops have a journal and there are over one hundred books on testing Still a full course on testing is offered only at a few universities mostly by professors who have a research interest in this area Apparently most professors would not have taken a course on electronic testing when they were students Other than the computer engineering curriculum being too crowded the major reason cited for the absence of a course on electronic testing is the lack of a suitable textbook For VLSI the foundation was provided by semiconductor device technology circuit design and electronic testing In a computer engineering curriculum therefore it is necessary that foundations should be taught before applications The field of VLSI has expanded to systems on a chip which include digital memory and mixed signal subsystems To our knowledge this is the first textbook to cover all three types of electronic circuits We have written this textbook for an undergraduate foundations course on electronic testing Obviously it is too voluminous for a one semester course and a teacher will have to select from the topics We did not restrict such freedom because the selection may depend upon the individual expertise and interests Besides there is merit in having a larger book that will retain its usefulness for the owner even after the completion of the course With equal tenacity we address the needs of three other groups of readers

**Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits** M. Bushnell, Vishwani Agrawal, 2014-01-15      **Essentials of Electronic Testing for Digital, Memory, and Mixed-signal VLSI Circuits** Michael Lee Bushnell, 2000      Integrated Circuit Test Engineering Ian A. Grout, 2005-08-22 Using the book and the software provided with it the reader can build his/her own tester arrangement to investigate key aspects of analog digital and mixed system circuits Plan of attack based on traditional testing circuit design and circuit manufacture allows the reader to appreciate a testing regime from the point of view of all the participating interests Worked examples based on theoretical bookwork practical experimentation and simulation exercises teach the reader how to test circuits thoroughly and effectively

**Cost Analysis of Electronic Systems** Peter Sandborn, 2013 Understanding the cost ramifications of design manufacturing and life cycle management decisions is of central importance to businesses associated with all types of electronic systems Cost Analysis of Electronic Systems contains carefully developed models and theory that practicing engineers can directly apply to the modeling of costs for real products and systems In addition this book brings to light and models many contributions to life cycle costs that practitioners are aware of but never had the tools or techniques to address quantitatively in the past Cost Analysis of Electronic Systems melds elements of traditional engineering economics with manufacturing process and life cycle cost management concepts to form a practical foundation for predicting the cost of electronic products and systems Various manufacturing cost analysis methods are addressed including process flow

parametric cost of ownership and activity based costing The effects of learning curves data uncertainty test and rework processes and defects are considered Aspects of system sustainment and life cycle cost modeling including reliability warranty burn in maintenance sparing and availability and obsolescence are treated Finally total cost of ownership of systems and return on investment are addressed Real life design scenarios from integrated circuit fabrication electronic systems assembly substrate fabrication and electronic systems management are used as examples of the application of the cost estimation methods developed within the book *Cost Analysis Of Electronic Systems (Second Edition)* Peter Sandborn, 2016-12-15 This book provides an introduction to the cost modeling for electronic systems that is suitable for advanced undergraduate and graduate students in electrical mechanical and industrial engineering and professionals involved with electronics technology development and management This book melds elements of traditional engineering economics with manufacturing process and life cycle cost management concepts to form a practical foundation for predicting the cost of electronic products and systems Various manufacturing cost analysis methods are addressed including process flow parametric cost of ownership and activity based costing The effects of learning curves data uncertainty test and rework processes and defects are considered Aspects of system sustainment and life cycle cost modeling including reliability warranty burn in maintenance sparing and availability and obsolescence are treated Finally total cost of ownership of systems return on investment cost benefit analysis and real options analysis are addressed *Reliability of Nanoscale Circuits and Systems* Miloš Stanisavljević, Alexandre Schmid, Yusuf Leblebici, 2010-10-20 This book is intended to give a general overview of reliability faults fault models nanotechnology nanodevices fault tolerant architectures and reliability evaluation techniques Additionally the book provides an in depth state of the art research results and methods for fault tolerance as well as the methodology for designing fault tolerant systems out of highly unreliable components **Hardware Protection through Obfuscation** Domenic Forte, Swarup Bhunia, Mark M. Tehranipoor, 2017-01-02 This book introduces readers to various threats faced during design and fabrication by today's integrated circuits ICs and systems The authors discuss key issues including illegal manufacturing of ICs or IC Overproduction insertion of malicious circuits referred as Hardware Trojans which cause in field chip system malfunction and reverse engineering and piracy of hardware intellectual property IP The authors provide a timely discussion of these threats along with techniques for IC protection based on hardware obfuscation which makes reverse engineering an IC design infeasible for adversaries and untrusted parties with any reasonable amount of resources This exhaustive study includes a review of the hardware obfuscation methods developed at each level of abstraction RTL gate and layout for conventional IC manufacturing new forms of obfuscation for emerging integration strategies split manufacturing 2.5D ICs and 3D ICs and on chip infrastructure needed for secure exchange of obfuscation keys arguably the most critical element of hardware obfuscation **Micro-Electro-Dot-Array Digital Microfluidic Biochips** Zipeng Li, Krishnendu Chakrabarty, Tsung-Yi Ho, Chen-Yi Lee, 2018-12-14 This book provides an

insightful guide to the design testing and optimization of micro electrode dot array MEDA digital microfluidic biochips The authors focus on the characteristics specific for MEDA biochips e g real time sensing and advanced microfluidic operations like lamination mixing and droplet shape morphing Readers will be enabled to enhance the automated design and use of MEDA and to develop a set of solutions to facilitate the full exploitation of design complexities that are possible with standard CMOS fabrication techniques The book provides the first set of design automation and test techniques for MEDA biochips The methods described in this book have been validated using fabricated MEDA biochips in the laboratory Readers will benefit from an in depth look at the MEDA platform and how to combine microfluidics with software e g applying biomolecular protocols to software controlled and cyberphysical microfluidic biochips

**Internet of Things** Bharat Bhusan, Sudhir Kumar Sharma, Bhuvan Unhelkar, Muhammad Fazal Ijaz, Lamia Karim, 2022-04-28 Today Internet of Things IoT is ubiquitous as it is applied in practice in everything from Industrial Control Systems ICS to e Health e commerce Cyber Physical Systems CPS smart cities smart parking healthcare supply chain management and many more Numerous industries academics alliances and standardization organizations make an effort on IoT standardization innovation and development But there is still a need for a comprehensive framework with integrated standards under one IoT vision Furthermore the existing IoT systems are vulnerable to huge range of malicious attacks owing to the massive numbers of deployed IoT systems inadequate data security standards and the resource constrained nature Existing security solutions are insufficient and therefore it is necessary to enable the IoT devices to dynamically counter the threats and save the system Apart from illustrating the diversified IoT applications this book also addresses the issue of data safekeeping along with the development of new security enhancing schemes such as blockchain as well as a range of other advances in IoT The reader will discover that the IoT facilitates a multidisciplinary approach dedicated to create novel applications and develop integrated solutions to build a sustainable society The innovative and fresh advances that demonstrate IoT and computational intelligence in practice are discussed in this book which will be helpful and informative for scientists research scholars academicians policymakers industry professionals government organizations and others This book is intended for a broad target audience including scholars of various generations and disciplines recognized scholars lecturers and professors and young researchers postgraduate and undergraduates who study the legal and socio economic consequences of the emergence and dissemination of digital technologies such as IoT Furthermore the book is intended for researchers developers and operators working in the field of IoT and eager to comprehend the vulnerability of the IoT paradigm The book will serve as a comprehensive guide for the advanced level students in computer science who are interested in understanding the severity and implications of the accompanied security issues in IoT Dr Bharat Bhusan is an Assistant Professor of Department of Computer Science and Engineering CSE at School of Engineering and Technology Sharda University Greater Noida India Prof Dr Sudhir Kumar Sharma is currently a Professor and Head of the Department of Computer Science Institute of Information Technology FACS

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**High Performance Memory Testing** R. Dean Adams, 2005-12-29 Are memory applications more critical than they have been in the past Yes but even more critical is the number of designs and the sheer number of bits on each design It is assured that catastrophes which were avoided in the past because memories were small will easily occur if the design and test engineers do not do their jobs very carefully High Performance Memory Testing Design Principles Fault Modeling and Self Test is based on the author's 20 years of experience in memory design memory reliability development and memory self test High Performance Memory Testing Design Principles Fault Modeling and Self Test is written for the professional and the researcher to help them understand the memories that are being tested

**Digital Timing Measurements** Wolfgang Maichen, 2006-10-03 As many circuits and applications now enter the Gigahertz frequency range accurate digital timing measurements have become crucial in the design verification characterization and application of electronic circuits To be successful in this endeavour an engineer needs a knowledge base covering instrumentation measurement techniques signal integrity jitter and timing concepts and statistics Very often even the most experienced digital test engineers while mastering some of those subjects lack systematic knowledge or experience in the high speed signal area Digital Timing Measurements gives a compact practice oriented overview on all those subjects The emphasis is on useable concepts and real life guidelines that can be readily put into practice with references to the underlying mathematical theory It unites in one place a variety of information relevant to high speed testing measurement signal fidelity and instrumentation

**Understanding Logic Locking** Kimia Zamiri Azar, Hadi Mardani Kamali, Farimah Farahmandi, Mark Tehranipoor, 2023-09-22 This book demonstrates the breadth and depth of IP protection through logic locking considering both attacker adversary and defender designer perspectives The authors draw a semi chronological picture of the evolution of logic locking during the last decade gathering and describing all the DO's and DON'Ts in this approach They describe simple to follow scenarios and guide readers to navigate identify threat models and design evaluation flow for further studies Readers will gain a comprehensive understanding of all fundamentals of logic locking

**A Designer's Guide to Built-In Self-Test** Charles E. Stroud, 2005-12-27 A recent technological advance is the art of designing circuits to test themselves referred to as a Built In Self Test This book is written from a designer's perspective and describes the major BIST approaches that have been proposed and implemented along with their advantages and limitations

**Power-Aware Testing and Test Strategies for Low Power Devices** Patrick Girard, Nicola Nicolici, Xiaoqing Wen, 2010-03-11 Managing the power consumption of circuits and systems is now considered one of the most important challenges for the semiconductor industry Elaborate power management strategies such as dynamic voltage scaling clock

gating or power gating techniques are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test and power aware test is therefore increasingly becoming a major consideration during design for test and test preparation for low power devices. This book explores existing solutions for power aware test and design for test of conventional circuits and systems and surveys test strategies and EDA solutions for testing low power devices.

**Proceeding of the Second International Conference on Microelectronics, Computing & Communication Systems (MCCS 2017)** Vijay Nath, Jyotsna Kumar Mandal, 2018-07-30. The volume presents high quality papers presented at the Second International Conference on Microelectronics Computing Communication Systems MCCS 2017. The book discusses recent trends in technology and advancement in MEMS and nanoelectronics, wireless communications, optical communication, instrumentation, signal processing, image processing, bioengineering, green energy, hybrid vehicles, environmental science, weather forecasting, cloud computing, renewable energy, RFID, CMOS sensors, actuators, transducers, telemetry systems, embedded systems, and sensor network applications. It includes original papers based on original theoretical, practical, experimental, simulations, development, application, measurement, and testing. The applications and solutions discussed in the book will serve as a good reference material for future works.

**SOC (System-on-a-Chip) Testing for Plug and Play Test Automation** Krishnendu Chakrabarty, 2013-04-17. System on a Chip SOC integrated circuits composed of embedded cores are now commonplace. Nevertheless, there remain several roadblocks to rapid and efficient system integration. Test development is seen as a major bottleneck in SOC design and manufacturing capabilities. Testing SOC is especially challenging in the absence of standardized test structures, test automation tools, and test protocols. In addition, long interconnects, high density, and high speed designs lead to new types of faults involving crosstalk and signal integrity. SOC System on a Chip Testing for Plug and Play Test Automation is an edited work containing thirteen contributions that address various aspects of SOC testing. SOC System on a Chip Testing for Plug and Play Test Automation is a valuable reference for researchers and students interested in various aspects of SOC testing.

**Testing Static Random Access Memories** Said Hamdioui, 2013-06-29. Testing Static Random Access Memories covers testing of one of the important semiconductor memories types; it addresses testing of static random access memories SRAMs, both single port and multi port. It contributes to the technical knowledge needed by those involved in memory testing: engineers and researchers. The book begins with outlining the most popular SRAM architectures. Then the description of realistic fault models based on defect injection and SPICE simulation are introduced. Thereafter, high quality and low cost test patterns, as well as test strategies for single port, two port, and any p port SRAMs are presented together with some preliminary test results showing the importance of the new tests in reducing DPM level. The impact of the port restrictions, e.g., read only ports, on the fault models, tests, and test strategies is also discussed. Features: Fault primitive based analysis of memory faults. A complete framework of and classification memory faults. A systematic way to develop optimal and high quality memory test

algorithms A systematic way to develop test patterns for any multi port SRAM Challenges and trends in embedded memory testing

**Embedded Processor-Based Self-Test** Dimitris Gizopoulos,A. Paschalis,Yervant Zorian,2013-03-09 Embedded Processor Based Self Test is a guide to self testing strategies for embedded processors Embedded processors are regularly used today in most System on Chips SoCs Testing of microprocessors and embedded processors has always been a challenge because most traditional testing techniques fail when applied to them This is due to the complex sequential structure of processor architectures which consists of high performance datapath units and sophisticated control logic for performance optimization Structured Design for Testability DfT and hardware based self testing techniques which usually have a non trivial impact on a circuit s performance size and power can not be applied without serious consideration and careful incorporation into the processor design Embedded Processor Based Self Test shows how the powerful embedded functionality that processors offer can be utilized as a self testing resource Through a discussion of different strategies the book emphasizes on the emerging area of Software Based Self Testing SBST SBST is based on the idea of execution of embedded software programs to perform self testing of the processor itself and its surrounding blocks in the SoC SBST is a low cost strategy in terms of overhead area speed power development effort and test application cost as it is applied using low cost low speed test equipment Embedded Processor Based Self Test can be used by designers DfT engineers test practitioners researchers and students working on digital testing and in particular processor and SoC test This book sets the framework for comparisons among different SBST methodologies by discussing key requirements It presents successful applications of SBST to a number of embedded processors of different complexities and instruction set architectures

*Digital System Test and Testable Design* Zainalabedin Navabi,2010-12-10 This book is about digital system testing and testable design The concepts of testing and testability are treated together with digital design practices and methodologies The book uses Verilog models and testbenches for implementing and explaining fault simulation and test generation algorithms Extensive use of Verilog and Verilog PLI for test applications is what distinguishes this book from other test and testability books Verilog eliminates ambiguities in test algorithms and BIST and DFT hardware architectures and it clearly describes the architecture of the testability hardware and its test sessions Describing many of the on chip decompression algorithms in Verilog helps to evaluate these algorithms in terms of hardware overhead and timing and thus feasibility of using them for System on Chip designs Extensive use of testbenches and testbench development techniques is another unique feature of this book Using PLI in developing testbenches and virtual testers provides a powerful programming tool interfaced with hardware described in Verilog This mixed hardware software environment facilitates description of complex test programs and test strategies



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