PBA Slack Prediction

b) Main Regression Model

Fully Connected Layer

Dropout Layer

Fully Connected Layer

c) Sub-Branch Regression Models
Used for training Phase; Removed in test phase

Launch Delay

Capture Delay

Data Delay

FC

FC

FC

a) Representation Learning

Launch Representation Learning

Capture Representation Learning

Data Representation Learning

Launch Path Features

Capture Path Features

Data Path Features

Input Sample

Great Lakes 4th Symposium On Vlsi Design Automation Of High Performance Vlsi Systems

Tak-Kei Lam,Wai-Chung Tang,Xing Wei,Yi Diao,David Yu-Liang Wu

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modules MCMs and other packaging methodologies Innovative technical papers in this book cover design optimization and physical partitioning global routing multi layer assignment timing driven interconnection design timing models clock and power design crosstalk reflection and simultaneous switching noise minimization yield optimization defect area minimization low power physical layout and design methodologies Two tutorial reviews review some of the most significant algorithms previously developed for the placement partitioning and signal integrity issues respectively The remaining articles review the trend of prime design automation algorithms to solve the above eight problems which arise in MCMs and other packages

Electronic Design Automation for IC System Design, Verification, and Testing Luciano Lavagno,Igor L. Markov,Grant Martin,Louis K. Scheffer,2017-12-19 The first of two volumes in the Electronic Design Automation for Integrated Circuits Handbook Second Edition Electronic Design Automation for IC System Design Verification and Testing thoroughly examines system level design microarchitectural design logic verification and testing Chapters contributed by leading experts authoritatively discuss processor modeling and design tools using performance metrics to select microprocessor cores for integrated circuit IC designs design and verification languages digital simulation hardware acceleration and emulation and much more New to This Edition Major updates appearing in the initial phases of the design flow where the level of abstraction keeps rising to support more functionality with lower non recurring engineering NRE costs Significant revisions reflected in the final phases of the design flow where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting edge applications and approaches realized in the decade since publication of the previous edition these are illustrated by new chapters on high level synthesis system on chip SoC block based design and back annotating system level models Offering improved depth and modernity Electronic Design Automation for IC System Design Verification and Testing provides a valuable state of the art reference for electronic design automation EDA students researchers and professionals **The Computer Engineering Handbook** Vojin G. Oklobdzija,2001-12-26 There is arguably no field in greater need of a comprehensive handbook than computer engineering The unparalleled rate of technological advancement the explosion of computer applications and the now in progress migration to a wireless world have made it difficult for engineers to keep up with all the developments in specialties outside their own References published only a few years ago are now sorely out of date The Computer Engineering Handbook changes all of that Under the leadership of Vojin Oklobdzija and a stellar editorial board some of the industry s foremost experts have joined forces to create what promises to be the definitive resource for computer design and engineering Instead of focusing on basic introductory material it forms a comprehensive state of the art review of the field s most recent achievements outstanding issues and future directions The world of computer engineering is vast and evolving so rapidly that what is cutting edge today may be obsolete in a few months While exploring the new developments trends and future directions of the field The Computer Engineering Handbook captures what is fundamental and of lasting value *Handbook*

of Algorithms for Physical Design Automation Charles J. Alpert,Dinesh P. Mehta,Sachin S. Sapatnekar,2008-11-12 The physical design flow of any project depends upon the size of the design the technology the number of designers the clock frequency and the time to do the design As technology advances and design styles change physical design flows are constantly reinvented as traditional phases are removed and new ones are added to accommodate changes in   Information Security Applications Ho-won Kim,Dooho Choi,2016-03-23 This book constitutes the thoroughly refereed post workshop proceedings of the 16th International Workshop on Information Security Applications WISA 2015 held on Jeju Island Korea in August 2015 The 35 revised full papers presented in this volume were carefully reviewed and selected from 78 submissions The papers are organized in topical sections such as hardware security cryptography side channel attacks and countermeasures security and threat analysis IoT security network security cryptography application security   **High-level Estimation and Exploration of Reliability for Multi-Processor System-on-Chip** Zheng Wang,Anupam Chattopadhyay,2017-06-23 This book introduces a novel framework for accurately modeling the errors in nanoscale CMOS technology and developing a smooth tool flow at high level design abstractions to estimate and mitigate the effects of errors The book presents novel techniques for high level fault simulation and reliability estimation as well as architecture level and system level fault tolerant designs It also presents a survey of state of the art problems and solutions offering insights into reliability issues in digital design and their cross layer countermeasures   **1995 IEEE TENCON** Institute of Electrical and Electronics Engineers. Region 10. Conference on Microelectronics and VLSI,1995   計算機アーキテクチャの基礎とワークブック ,1997   **Directory of Published Proceedings** ,2001   *Fourth Great Lakes Symposium on VLSI* ,1994   Conference Proceedings ,1995   Three-Dimensional Integrated Circuit Design Yuan Xie,Jingsheng Jason Cong,Sachin Sapatnekar,2009-12-02 We live in a time of great change In the electronics world the last several decades have seen unprecedented growth and advancement described by Moore s law This observation stated that transistor density in integrated circuits doubles every 1 5 2 years This came with the simultaneous improvement of individual device perf mance as well as the reduction of device power such that the total power of the resulting ICs remained under control No trend remains constant forever and this is unfortunately the case with Moore s law The trouble began a number of years ago when CMOS devices were no longer able to proceed along the classical scaling trends Key device parameters such as gate oxide thickness were simply no longer able to scale As a result device o state currents began to creep up at an alarming rate These continuing problems with classical scaling have led to a leveling off of IC clock speeds to the range of several GHz Of course chips can be clocked higher but the thermal issues become unmanageable This has led to the recent trend toward microprocessors with mul ple cores each running at a few GHz at the most The goal is to continue improving performance via parallelism by adding more and more cores instead of increasing speed The challenge here is to ensure that general purpose codes can be ef ciently parallelized There is another potential solution to the problem of how to improve CMOS technology

performance three dimensional integrated circuits 3D ICs **Boolean Circuit Rewiring** Tak-Kei Lam,Wai-Chung Tang,Xing Wei,Yi Diao,David Yu-Liang Wu,2016-01-11 Demonstrates techniques which will allow rewiring rates of over 95% enabling adoption of deep sub micron chips for industrial applications Logic synthesis is an essential part of the modern digital IC design process in semi conductor industry This book discusses a logic synthesis technique called rewiring and its latest technical advancement in term of rewirability Rewiring technique has surfaced in academic research since 1993 and there is currently no book available on the market which systematically and comprehensively discusses this rewiring technology The authors cover logic transformation techniques with concentration on rewiring For many decades the effect of wiring on logic structures has been ignored due to an ideal view of wires and their negligible role in the circuit performance However in today s semiconductor technology wiring is the major player in circuit performance degeneration and logic synthesis engines can be improved to deal with this through wire based transformations This book introduces the automatic test pattern generation ATPG based rewiring techniques which are recently active in the realm of logic synthesis verification of VLSI SOC designs Unique comprehensive coverage of semiconductor rewiring techniques written by leading researchers in the field Provides complete coverage of rewiring from an introductory to intermediate level Rewiring is explained as a flexible technique for Boolean logic synthesis introducing the concept of Boolean circuit transformation and testing with examples Readers can directly apply the described techniques to real world VLSI design issues Focuses on the automatic test pattern generation ATPG based rewiring methods although some non ATPG based rewiring methods such as graph based alternative wiring GBAW and set of pairs of functions to be distinguished SPFD based rewiring are also discussed A valuable resource for researchers and postgraduate students in VLSI and SoC design as well as digital design engineers EDA software developers and design automation experts that specialize in the synthesis and optimization of logical circuits

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