

VLSI TESTING

積體電路測試

CHAPTER 1 INTRODUCTION TO VLSI TESTING

賴秉樞

PING-LIANG LAI



Introduction To Vlsi Testing

EDFAS Desk Reference Committee



Introduction To Vlsi Testing:

Introduction to VLSI Testing Robert J. Feugate, Steven M. McIntyre, 1988 **VLSI Testing** Stanley Leonard Hurst, 1998 Hurst an editor at the Microelectronics Journal analyzes common problems that electronics engineers and circuit designers encounter while testing integrated circuits and the systems in which they are used and explains a variety of solutions available for overcoming them in both digital and mixed circuits Among his topics are faults in digital circuits generating a digital test pattern signatures and self tests structured design for testability testing structured digital circuits and microprocessors and financial aspects of testing The self contained reference is also suitable as a textbook in a formal course on the subject Annotation copyrighted by Book News Inc Portland OR *Introduction to VLSI Testing* Robert J. Feugate (jr.), Steven M. McIntyre, 1988 **VLSI Test Principles and Architectures** Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen, 2006-08-14 This book is a comprehensive guide to new DFT methods that will show the readers how to design a testable and quality product drive down test cost improve product quality and yield and speed up time to market and time to volume Most up to date coverage of design for testability Coverage of industry practices commonly found in commercial DFT tools but not discussed in other books Numerous practical examples in each chapter illustrating basic VLSI test principles and DFT architectures **On-Line Testing for VLSI** Michael Nicolaidis, Yervant Zorian, Dhiraj Pradhan, 2013-03-09 Test functions fault detection diagnosis error correction repair etc that are applied concurrently while the system continues its intended function are defined as on line testing In its expanded scope on line testing includes the design of concurrent error checking subsystems that can be themselves self checking fail safe systems that continue to function correctly even after an error occurs reliability monitoring and self test and fault tolerant designs On Line Testing for VLSI contains a selected set of articles that discuss many of the modern aspects of on line testing as faced today The contributions are largely derived from recent IEEE International On Line Testing Workshops Guest editors Michael Nicolaidis Yervant Zorian and Dhiraj Pradhan organized the articles into six chapters In the first chapter the editors introduce a large number of approaches with an expanded bibliography in which some references date back to the sixties On Line Testing for VLSI is an edited volume of original research comprising invited contributions by leading researchers **Introduction to Advanced System-on-Chip Test Design and Optimization** Erik Larsson, 2006-03-30 SOC test design and its optimization is the topic of Introduction to Advanced System on Chip Test Design and Optimization It gives an introduction to testing describes the problems related to SOC testing discusses the modeling granularity and the implementation into EDA electronic design automation tools The book is divided into three sections i test concepts ii SOC design for test and iii SOC test applications The first part covers an introduction into test problems including faults fault types design flow design for test techniques such as scan testing and Boundary Scan The second part of the book discusses SOC related problems such as system modeling test conflicts power consumption test access mechanism design test scheduling and defect oriented

scheduling Finally the third part focuses on SOC applications such as integrated test scheduling and TAM design defect oriented scheduling and integrating test design with the core selection process

Principles of Testing Electronic Systems Samiha Mourad,Yervant Zorian,2000-07-25 A pragmatic approach to testing electronic systems As we move ahead in the electronic age rapid changes in technology pose an ever increasing number of challenges in testing electronic products Many practicing engineers are involved in this arena but few have a chance to study the field in a systematic way learning takes place on the job By covering the fundamental disciplines in detail Principles of Testing Electronic Systems provides design engineers with the much needed knowledge base Divided into five major parts this highly useful reference relates design and tests to the development of reliable electronic products shows the main vehicles for design verification examines designs that facilitate testing and investigates how testing is applied to random logic memories FPGAs and microprocessors Finally the last part offers coverage of advanced test solutions for today s very deep submicron designs The authors take a phenomenological approach to the subject matter while providing readers with plenty of opportunities to explore the foundation in detail Special features include An explanation of where a test belongs in the design flow Detailed discussion of scan path and ordering of scan chains BIST solutions for embedded logic and memory blocks Test methodologies for FPGAs A chapter on testing system on a chip Numerous references

Designer's Guide to Testable Asic Devices Wayne M. Needham,1991-01-10 While making up a larger percentage of the total number of designs produced each year ASICs present special problems for system designers in the area of testing because each design is complex and unique This book shows readers how to apply basic test techniques to ASIC design details the impact of ASIC testability on total system cost and performance and reviews the commercial test systems that are currently available Annotation copyrighted by Book News Inc Portland OR

IDDQ Testing of VLSI Circuits Ravi K. Gulati,Charles F. Hawkins,2012-12-06 Power supply current monitoring to detect CMOS IC defects during production testing quietly laid down its roots in the mid 1970s Both Sandia Labs and RCA in the United States and Philips Labs in the Netherlands practiced this procedure on their CMOS ICs At that time this practice stemmed simply from an intuitive sense that CMOS ICs showing abnormal quiescent power supply current IDDQ contained defects Later this intuition was supported by data and analysis in the 1980s by Levi RACD Malaiya and Su SUNY Binghamton Soden and Hawkins Sandia Labs and the University of New Mexico Jacomino and co workers Laboratoire d Automatique de Grenoble and Maly and co workers Carnegie Mellon University Interest in IDDQ testing has advanced beyond the data reported in the 1980s and is now focused on applications and evaluations involving larger volumes of ICs that improve quality beyond what can be achieved by previous conventional means In the conventional style of testing one attempts to propagate the logic states of the suspended nodes to primary outputs This is done for all or most nodes of the circuit For sequential circuits in particular the complexity of finding suitable tests is very high In comparison the IDDQ test does not observe the logic states but measures the integrated current that leaks through all gates In other words it is like

measuring a patient's temperature to determine the state of health. Despite perceived advantages during the years that followed its initial announcements, skepticism about the practicality of IDDQ testing prevailed. The idea, however, provided a great opportunity to researchers. New results on test generation, fault simulation, design for testability, built-in self-test, and diagnosis for this style of testing have since been reported. After a decade of research, we are definitely closer to practice.

Understanding Logic Locking Kimia Zamiri Azar, Hadi Mardani Kamali, Farimah Farahmandi, Mark

Tehranipour, 2023-09-22 This book demonstrates the breadth and depth of IP protection through logic locking, considering both attacker/adversary and defender/designer perspectives. The authors draw a semi-chronological picture of the evolution of logic locking during the last decade, gathering and describing all the DO's and DON'Ts in this approach. They describe simple-to-follow scenarios and guide readers to navigate, identify threat models, and design evaluation flow for further studies. Readers will gain a comprehensive understanding of all fundamentals of logic locking. *Nanometer Technology Designs*

Nisar Ahmed, 2010-02-26 Adopting new fabrication technologies not only provides higher integration and enhances performance but also increases the types of manufacturing defects. With design size in millions of gates and working frequency in GHz, timing-related defects have become a high proportion of the total chip defects. For nanometer technology designs, the stuck-at-fault test alone cannot ensure a high quality level of chips. At speed tests using the transition fault model, has become a requirement in technologies below 180nm. Traditional at-speed test methods cannot guarantee high quality test results as they face many new challenges: Supply noise including IR drop, ground bounce, and Ldi/dt effects on chip performance; high test pattern volume; low fault defect coverage; small delay defect test pattern generation; high cost of test implementation and application; and utilizing low cost testers are among these challenges. This book discusses these challenges in detail and proposes new techniques and methodologies to improve the overall quality of the transition fault test.

Introduction to Design VLSI Testing, 2003

Rapid Reliability Assessment of VLSICs A.P. Dorey, B.K.

Jones, A.M.D. Richardson, Y.Z. Xu, 2012-12-06 The increasing application of integrated circuits in situations where high reliability is needed places a requirement on the manufacturer to use methods of testing to eliminate devices that may fail on service. One possible approach that is described in this book is to make precise electrical measurements that may reveal those devices more likely to fail. The measurements assessed are of analog circuit parameters which, based on a knowledge of failure mechanisms, may indicate a future failure. To incorporate these tests into the functional listing of very large scale integrated circuits, consideration has to be given to the sensitivity of the tests where small numbers of devices may be defective in a complex circuit. In addition, the tests ideally should require minimal extra test time. A range of tests has been evaluated and compared with simulation used to assess the sensitivity of the measurements. Other work in the field is fully referenced at the end of each chapter. The team at Lancaster responsible for this book wish to thank the Alvey directorate and SERe for the necessary support and encouragement to publish our results. We would also like to thank John Henderson

recently retired from the British Telecom Research Laboratories for his cheerful and enthusiastic encouragement Trevor Ingham now in New Zealand is thanked for his early work on the project

Integrated Circuit Quality and Reliability Eugene R. Hnatek, 2018-10-03 Examines all important aspects of integrated circuit design fabrication assembly and test processes as they relate to quality and reliability This second edition discusses in detail the latest circuit design technology trends the sources of error in wafer fabrication and assembly avenues of contamination new IC packaging methods new in line process monitors and test structures and more This work should be useful to electrical and electronics quality and reliability and industrial engineers computer scientists integrated circuit manufacturers and upper level undergraduate graduate and continuing education students in these disciplines

Introduction to Hardware Security and Trust Mohammad Tehranipoor, Cliff Wang, 2011-09-22 This book provides the foundations for understanding hardware security and trust which have become major concerns for national security over the past decade Coverage includes security and trust issues in all types of electronic devices and systems such as ASICs COTS FPGAs microprocessors DSPs and embedded systems This serves as an invaluable reference to the state of the art research that is of critical significance to the security of and trust in modern society's microelectronic supported infrastructures

Microelectronics Failure Analysis Desk Reference, Seventh Edition Tejinder Gandhi, 2019-11-01 The Electronic Device Failure Analysis Society proudly announces the Seventh Edition of the Microelectronics Failure Analysis Desk Reference published by ASM International The new edition will help engineers improve their ability to verify isolate uncover and identify the root cause of failures Prepared by a team of experts this updated reference offers the latest information on advanced failure analysis tools and techniques illustrated with numerous real life examples This book is geared to practicing engineers and for studies in the major area of power plant engineering For non metallurgists a chapter has been devoted to the basics of material science metallurgy of steels heat treatment and structure property correlation A chapter on materials for boiler tubes covers composition and application of different grades of steels and high temperature alloys currently in use as boiler tubes and future materials to be used in supercritical ultra supercritical and advanced ultra supercritical thermal power plants A comprehensive discussion on different mechanisms of boiler tube failure is the heart of the book Additional chapters detailing the role of advanced material characterization techniques in failure investigation and the role of water chemistry in tube failures are key contributions to the book

Microelectronics Failure Analysis EDFAS Desk Reference Committee, 2011 Includes bibliographical references and index

Test and Diagnosis for Small-Delay Defects Mohammad Tehranipoor, Ke Peng, Krishnendu Chakrabarty, 2011-09-08 This book will introduce new techniques for detecting and diagnosing small delay defects in integrated circuits Although this sort of timing defect is commonly found in integrated circuits manufactured with nanometer technology this will be the first book to introduce effective and scalable methodologies for screening and diagnosing small delay defects including important parameters such as process variations crosstalk and power supply noise

Tutorial Test

Generation for VLSI Chips Vishwani D. Agrawal, 1988

Semiconductor International , 1988

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