Introduction

- ## Architecture Synthesis

  - ### Behavioral description

    exploration of design space

  - ### RTL description (structural view of datapath
    ### + logic-level specification of control unit)

  - ### Datapath

    - interconnection of resources

  - ### Resource

    - functional resource (ALU, adder, multiplier, ...)

    - memory resource (register, RAM, ROM, ...)

    - interface resource (bus, steering logic, I/O pad, ...)

Logic And Architecture Synthesis

Hubert Kaeslin

Logic And Architecture Synthesis:

   Logic and Architecture Synthesis Gabrièle Saucier,Anne Mignotte,1995 This book describes several methods and systems solving one of the highlighted problems within computer aided design namely architectural and logic synthesis The book emphasises the most recent technologies in high level synthesis concentrating on applicative studies and practical constraints or criteria during synthesis Logic and Architecture Synthesis concentrates on the practical problems involving automatic synthesis of designs It is essential reading for researchers and CAD Managers working in this area *Logic and Architecture Synthesis* Gabriele Saucier,Anne Mignotte,1995-07-31 This book describes several methods and systems solving one of the highlighted problems within computer aided design namely architectural and logic synthesis The book emphasises the most recent technologies in high level synthesis concentrating on applicative studies and practical constraints or criteria during synthesis Logic and Architecture Synthesis concentrates on the practical problems involving automatic synthesis of designs It is essential reading for researchers and CAD Managers working in this area **Field-Programmable Logic: Architectures, Synthesis and Applications** Reiner W. Hartenstein,1994-08-24 This volume contains the proceedings of the 4th International Workshop on Field Programmable Logic and Applications FPL 94 held in Prague Czech Republic in September 1994 The growing importance of field programmable devices is substantiated by the remarkably high number of 116 submissions for FPL 94 from them the revised versions of 40 full papers and 24 high quality poster presentations were accepted for inclusion in this volume Among the topics treated are testing layout synthesis tools compilation research and CAD trade offs and experience innovations and smart applications FPGA based computer architectures high level design prototyping and ASIC emulators commercial devices new tools CCMs and HW SW co design modelers educational experience and novel architectures Logic and Architecture Synthesis for Silicon Compilers Gabrièle Saucier,Paul Michael McLellan,1989 VLSI synthesis is a subject that is moving rapidly from the research laboratory into the industrial environment and it is generally accepted that synthesis will gradually become the dominant design technique surpassing conventional manual techniques This book provides a timely overview on the various systems for logical and architectural synthesis for VLSI It discusses the algorithms and techniques necessary for a synthesis system that is competitive with current design techniques for integrated circuits The book covers both low level logic synthesis techniques and higher level architectural techniques both of which are increasing in practical importance since they will form the basis of the next generation of CAD software for integrated circuits Three main topics are addressed The first concerns two level and multi level synthesis It includes PLA and PAL implementation as well as standard cell and compiled cell based synthesis The second concerns controller synthesis with emphasis on optimisation methods The third deals with high level synthesis resource allocation scheduling as applied to DSP systems and processors consisting of controllers and data paths **Compilation Techniques for Reconfigurable Architectures** João M.P. Cardoso,Pedro C. Diniz,2011-04-02 The extreme exibility of recon gurable

architectures and their performance pot tial have made them a vehicle of choice in a wide range of computing domains from rapid circuit prototyping to high performance computing The increasing availab ity of transistors on a die has allowed the emergence of recon gurable architectures with a large number of computing resources and interconnection topologies To ploit the potential of these recon gurable architectures programmers are forced to map their applications typically written in high level imperative programming l guages such as C or MATLAB to hardware oriented languages such as VHDL or Verilog In this process they must assume the role of hardware designers and software programmers and navigate a maze of program transformations mapping and synthesis steps to produce ef cient recon gurable computing implementations The richness and sophistication of any of these application mapping steps make the mapping of computations to these architectures an increasingly daunting process It is thus widely believed that automatic compilation from high level programming languages is the key to the success of recon gurable computing This book describes a wide range of code transformations and mapping te niques for programs described in high level programming languages most tably imperative languages to recon gurable architectures **Switching and Finite Automata Theory** Zvi Kohavi,Niraj K. Jha,2010 Understand the structure behavior and limitations of logic machines with this thoroughly updated third edition Many new topics are included such as CMOS gates logic synthesis logic design for emerging nanotechnologies digital system testing and asynchronous circuit design to bring students up to speed with modern developments The intuitive examples and minimal formalism of the previous edition are retained giving students a text that is logical and easy to follow yet rigorous Kohavi and Jha begin with the basics and then cover combinational logic design and testing before moving on to more advanced topics in finite state machine design and testing Theory is made easier to understand with 200 illustrative examples and students can test their understanding with over 350 end of chapter review questions **Parallel and Distributed Processing** José D. P. Rolim,1999-03-30 This book constitutes the refereed proceedings of 11 IPPS SPDP 98 Workshops held in conjunction with the 13th International Parallel Processing Symposium and the 10th Symposium on Parallel and Distributed Processing in San Juan Puerto Rico USA in April 1999 The 126 revised papers presented were carefully selected from a wealth of papers submitted The papers are organised in topical sections on biologically inspired solutions to parallel processing problems High Level Parallel Programming Models and Supportive Environments Biologically Inspired Solutions to Parallel Processing Parallel and Distributed Real Time Systems Run Time Systems for Parallel Programming Reconfigurable Architectures Java for Parallel and Distributed Computing Optics and Computer Science Solving Irregularly Structured Problems in Parallel Personal Computer Based Workstation Networks Formal Methods for Parallel Programming Embedded HPC Systems and Applications Pattern Recognition Technologies and Applications: Recent Advances Verma, Brijesh,Blumenstein, Michael,2008-06-30 The nature of handwriting in our society has significantly altered over the ages due to the introduction of new technologies such as computers and the World Wide Web With increases in the amount of signature verification needs state of the art

internet and paper based automated recognition methods are necessary Pattern Recognition Technologies and Applications Recent Advances provides cutting edge pattern recognition techniques and applications Written by world renowned experts in their field this easy to understand book is a must have for those seeking explanation in topics such as on and offline handwriting and speech recognition signature verification and gender classification *Domain-Specific Processors* Shuvra S. Bhattacharyya,Ed F. Deprettere,Jörgen Teich,2003-11-11 Ranging from low level application and architecture optimizations to high level modeling and exploration concerns this authoritative reference compiles essential research on various levels of abstraction appearing in embedded systems and software design It promotes platform based design for improved system implementation and modeling and enhanced *Logic and Architecture Synthesis* Petra Michel,Gabrièle Saucier,1991 The papers presented in this book cover the whole spectrum from high level synthesis to technology mapping including an overview of fifty years of logic synthesis and asking whether high level synthesis is practical at all The reader will undoubtedly be left with the impression that though the field of synthesis has made considerable progress in the last few years there are still many problems to be dealt with DSP Integrated Circuits Lars Wanhammar,1999-02-24 DSP Integrated Circuits establishes the essential interface between theory of digital signal processing algorithms and their implementation in full custom CMOS technology With an emphasis on techniques for co design of DSP algorithms and hardware in order to achieve high performance in terms of throughput low power consumption and design effort this book provides the professional engineer researcher and student with a firm foundation in the theoretical as well as the practical aspects of designing high performance DSP integrated circuits Centered around three design case studies DSP Integrated Circuits thoroughly details a high performance FFT processor a 2 D Discrete Cosine Transform for HDTV and a wave digital filter for interpolation of the sampling frequency The case studies cover the essential parts of the design process in a top down manner from specification of algorithm design and optimization scheduling of operations synthesis of optimal architectures realization of processing elements to the floor planning of the integrated circuit Details the theory and design of digital filters particularly wave digital filters multi rate digital filters fast Fourier transforms FFT s and discrete cosine transforms DCT s Follows three complete real world case studies throughout the book Provides complete coverage of finite word length effects in DSP algorithms In depth survey of the computational properties of DSP algorithms and their mapping to optimal architectures Outlines DSP architectures and parallel bit serial and distributed arithmetic Presents the design process in a top down manner and incorporates numerous problems and solutions *Design of Embedded Control Systems* Marian Andrzej Adamski,Andrei Karatkevich,Marek Wegrzyn,2006-11-22 A set of original results in the eld of high level design of logical control devices and systems is presented in this book These concern different aspects of such important and long term design problems including the following which seem to be the main ones First the behavior of a device under design must be described properly and some adequate formal language should be chosen for that Second effective

algorithmsshouldbeusedforcheckingthepreparedddescriptionforcorrectness foritssyntacticandsemanticveri cationattheinitialbehaviorlevel Third the problem of logic circuit implementation must be solved using some concrete technological base ef cient methods of logic synthesis test and veri cation should be developed for that Fourth the task of the communication between the control device and controlled objects and maybe between different control devices waitsforitssolution Alltheseproblemsarehardenoughandcannotbe successfully solved without ef cient methods and algorithms oriented toward computer implementation Some of these are described in this book The languages used for behavior description have been descended usually from two well known abstract models which became classic Petri nets and nite state machines FSMs Anyhow more detailed versions are developed and described in the book which enable to give more complete information concerningspeci cqualitiesoftheregardedsystems Forexample themodelof parallelautomatonispresented whichunliketheconventional niteautomaton can be placed simultaneously into several places calledpartial As a base for circuit implementation of control algorithms FPGA is accepted in majority of cases **VLSI: Systems on a Chip** Luis Miguel Silveira,Srinivas Devadas,Ricardo A. Reis,2013-11-11 For over three decades now silicon capacity has steadily been doubling every year and a half with equally staggering improvements continuously being observed in operating speeds This increase in capacity has allowed for more complex systems to be built on a single silicon chip Coupled with this functionality increase speed improvements have fueled tremendous advancements in computing and have enabled new multi media applications Such trends aimed at integrating higher levels of circuit functionality are tightly related to an emphasis on compactness in consumer electronic products and a widespread growth and interest in wireless communications and products These trends are expected to persist for some time as technology and design methodologies continue to evolve and the era of Systems on a Chip has definitely come of age While technology improvements and spiraling silicon capacity allow designers to pack more functions onto a single piece of silicon they also highlight a pressing challenge for system designers to keep up with such amazing complexity To handle higher operating speeds and the constraints of portability and connectivity new circuit techniques have appeared Intensive research and progress in EDA tools design methodologies and techniques is required to empower designers with the ability to make efficient use of the potential offered by this increasing silicon capacity and complexity and to enable them to design test verify and build such systems **Correct Hardware Design and Verification Methods** George J. Milne,Laurence Pierre,1993-05-12 These proceedings contain the papers presented at the Advanced Research Working Conference on Correct Hardware Design Methodologies held in Arles France in May 1993 and organized by the ESPRIT Working Group 6018 CHARME 2and the Universit de Provence Marseille in cooperation with IFIP Working Group 10 2 Formal verification is emerging as a plausible alternative to exhaustive simulation for establishing correct digital hardware designs The validation of functional and timing behavior is a major bottleneck in current VLSI design systems slowing the arrival of products in the marketplace with its associated increase in cost From

being a predominantly academic area of study until a few years ago formal design and verification techniques are now beginning to migrate into industrial use As we are now witnessing an increase in activity in this area in both academia and industry the aim of this working conference was to bring together researchers and users from both communities

Computer Systems: Architectures, Modeling, and Simulation Andy Pimentel,Stamatis Vassiliadis,2004-07-05 This book constitutes the refereed proceedings of the 4th International Workshop on Systems Architectures Modeling and Simulation SAMOS 2004 held in Samos Greece on July 2004 Besides the SAMOS 2004 proceedings the book also presents 19 revised papers from the predecessor workshop SAMOS 2003 The 55 revised full papers presented were carefully reviewed and selected for inclusion in the book The papers are organized in topical sections on reconfigurable computing architectures and implementation and systems modeling and simulation   VLSI: Integrated Systems on Silicon Ricardo A. Reis,Luc Claesen,2013-06-05 This book contains the papers that have been presented at the ninth Very Large Scale Integrated Systems conference VLSI 97 that is organized biannually by IFIP Working Group 10 5 It took place at Hotel Serra Azul in Gramado Brazil from 26 30 August 1997 Previous conferences have taken place in Edinburgh Trondheim Vancouver Munich Grenoble and Tokyo The papers in this book report on all aspects of importance to the design of the current and future integrated systems The current trend towards the realization of versatile Systems on a Chip require attention of embedded hardware software systems dedicated ASIC hardware sensors and actuators mixed analog digital design video and image processing low power battery operation and wireless communication The papers as presented in Jhis book have been organized in two tracks where one is dealing with VLSI System Design and Applications and the other presents VLSI Design Methods and CAD The following topics are addressed VLSI System Design and Applications Track VLSI for Video and Image Processing Microsystem and Mixed mode design Communication And Memory System Design Cow voltage Low power Analog Circuits High Speed Circuit Techniques Application Specific DSP Architectures VLSI Design Methods and CAD Track Specification and Simulation at System Level Synthesis and Technology Mapping CAD Techniques for Low Power Design Physical Design Issues in Sub micron Technologies Architectural Design and Synthesis Testing in Complex Mixed Analog and Digital Systems   **Architecture Design and Validation Methods** Egon Börger,2012-12-06 This book grew out of material which was taught at the International Summer School on Architecture Design and Validation Methods held June 23 July 5 1997 on the Island of Lipari and directed to graduate students and young researchers Since then the course notes have been completely elaborated and extended and additional chapters have been added so that this book offers a comprehensive presentation of the state of the art which leads the reader to the forefront of the current research in the area The chapters each of which was written by a group of eminent special ists in the field are self contained and can be read independently of each other They cover the wide range of theoretical and practical methods which currently used for the specification design validation and verification of are hardware software architectures Synthesis methods are the subject of the first three

chapters The chapter on Modeling and Synthesis of Behavior Control and Data Flow focusses on techniques above the register transfer level The chapter on Cell Based Logic Optimizations concentrates on methods that interface logic design with phys ical design in particular on techniques for cell library binding the back end of logic synthesis The chapter on A Design Flow for Performance Planning presents new paradigms for iteration free synthesis where global wire plans for meeting timing constraints already appear at the conceptual design stage even before fixing the functionality of the blocks in the plan **Digital Integrated Circuit Design** Hubert Kaeslin,2008-04-28 This practical tool independent guide to designing digital circuits takes a unique top down approach reflecting the nature of the design process in industry Starting with architecture design the book comprehensively explains the why and how of digital circuit design using the physics designers need to know and no more VLSI Design Methodologies for Digital Signal Processing Architectures Magdy A. Bayoumi,2012-12-06 Designing VLSI systems represents a challenging task It is a transfonnation among different specifications corresponding to different levels of design abstraction behavioral stntctural and physical The behavioral level describes the functionality of the design It consists of two components static and dynamic The static component describes operations whereas the dynamic component describes sequencing and timing The structural level contains infonnation about components control and connectivity The physical level describes the constraints that should be imposed on the floor plan the placement of components and the geometry of the design Constraints of area speed and power are also applied at this level To implement such multilevel transfonnation a design methodology should be devised taking into consideration the constraints limitations and properties of each level The mapping process between any of these domains is non isomorphic A single behavioral component may be transfonned into more than one structural component Design methodologies are the most recent evolution in the design automation era which started off with the introduction and subsequent usage of module generation especially for regular structures such as PLA s and memories A design methodology should offer an integrated design system rather than a set of separate unrelated routines and tools A general outline of a desired integrated design system is as follows Decide on a certain unified framework for all design levels Derive a design method based on this framework Create a design environment to implement this design method **Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology** Luciano Lavagno,Igor L. Markov,Grant Martin,Louis K. Scheffer,2017-02-03 The second of two volumes in the Electronic Design Automation for Integrated Circuits Handbook Second Edition Electronic Design Automation for IC Implementation Circuit Design and Process Technology thoroughly examines real time logic RTL to GDSII a file format used to transfer data of semiconductor physical layout design flow analog mixed signal design physical verification and technology computer aided design TCAD Chapters contributed by leading experts authoritatively discuss design for manufacturability DFM at the nanoscale power supply network design and analysis design modeling and much more New to This Edition Major updates appearing in the initial phases of the design flow where

the level of abstraction keeps rising to support more functionality with lower non recurring engineering NRE costs Significant revisions reflected in the final phases of the design flow where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting edge applications and approaches realized in the decade since publication of the previous edition these are illustrated by new chapters on 3D circuit integration and clock design Offering improved depth and modernity Electronic Design Automation for IC Implementation Circuit Design and Process Technology provides a valuable state of the art reference for electronic design automation EDA students researchers and professionals

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