Logic Synthesis for Field-Programmable Gate Arrays

Ting-Ting Hwang, Robert Michael Owens, Mary Jane Irwin, *Fellow, IEEE*, and Kuo Hua Wang

Abstract—In this paper, we consider the problem of configuring Field Programmable Gate Arrays (FPGA's) so that some given function is computed by the device. Obtaining the information necessary to configure a FPGA entails both logic synthesis and logic embedding. Due to the very constrained nature of the embedding process, this problem differs from traditional multilevel logic synthesis in that the structure [illegible] of the synthesized logic is much more important. Furthermore, a metric-like literal count is much less important. We present a communication complexity-based decomposition technique that appears to be more suitable for FPGA synthesis than other multilevel logic synthesis methods. The key is that our logic optimization technique based on reducing communication complexity is good enough to allow a simple technology mapping to work well for FPGA devices.

I. INTRODUCTION

FIELD PROGRAMMABLE Gate Arrays (FPGA's) are a recent technology that provides more programmability in the field. Because of their very short turnaround time and low manufacturing cost, there has been an increasing interest in system prototyping using FPGA's. One important class is the RAM-based FPGA (also called "look-up table FPGA's"). A novel feature of these devices is that each basic block can implement any logic function that satisfies the I/O constraints of the basic block. The interconnections between the basic blocks consist of metal segments joined by program controlled pass transistors. From the above description, we can see that two features of FPGA's that the logic synthesis process has to take into consideration are 1) functions are implemented using look-up tables (LUT) and 2) restricted interconnections. To configure a FPGA requires programming both the LUT and the interconnect. In many ways, configuring a FPGA is similar to the traditional custom VLSI synthesis process. Given a logic function to be realized, an equivalent multilevel logic description is first generated. The synthesized description is technology mapped, and finally, the mapped description is embedded in circuitry.

However, even though similar in approach, traditional logic synthesis tools may not be well suited for FPGA configuration for the following two reasons. First, because each LUT can emulate any k-input gate, where k is the input limit of a LUT function unit, it is possible for large expressions and/or subexpressions of the synthesized description to be mapped to a single LUT if the expression/subexpression involves k or fewer different variables. For example, consider the case where basic block is a 16-bit, 4 input LUT and let $f_1 = abcde$ and $f_2 = abcd + \bar{a}\bar{b}\bar{c}\bar{d}$. Although in terms of literal count f_2 is more complex than f_1, f_2 can be realized using one 4-input LUT while f_1 would need two 4-input LUT's. This implies that traditional logic synthesis that focuses on minimizing the number of literals may not be the best approach for FPGA's. The processes of logic synthesis and technology mapping for FPGA's should not be decoupled. Second, because of the FPGA's structure, embedding the mapped description enjoys less flexibility than in traditional custom VLSI synthesis. This implies that how well a mapped description can be embedded in a FPGA can be very dependent on the structure of the mapped description. To embed a general circuit graph is more difficult than embedding a restricted circuit graph (e.g., a tree). All of this means that how good the final configuration is will be much more dependent on the structure of the synthesized description than in traditional VLSI synthesis.

We present a logic synthesis technique that overcomes these two limitations. Our technique is based on minimizing the communication complexity of the synthesized circuit rather than concentrating on literal count. The remainder of this paper is organized as follows. In Section II, we review the communication-based logic synthesis technique that is used to construct a global, technology-independent structure. In Section III, we show that communication-based logic synthesis is more suitable for configuring FPGA's. We then present an algorithm for mapping technology independent logic to FPGA's in Section IV. Some benchmarking results and comparisons are given in Section V.

II. COMMUNICATION COMPLEXITY-BASED LOGIC SYNTHESIS

In this section, we will give an overview of communication complexity based logic synthesis. A detailed description can be found in [11]. Succinctly, communication-complexity-based logic synthesis can be stated as follows. For some function

$$y = f(x), \quad f: B^n \to B^m, \quad B = \{0, 1\}$$

where the elements of x are the n binary inputs and the elements of y are the m binary outputs of the function and some partitioning (x_1, x_2) of x, let S_1, S_2 and S_c be a set of

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    Logic Synthesis for Field-Programmable Gate Arrays Rajeev Murgai,Robert K. Brayton,Alberto L. Sangiovanni-Vincentelli,2012-12-06 Short turnaround has become critical in the design of electronic systems Software programmable components such as microprocessors and digital signal processors have been used extensively in such systems since they allow rapid design revisions However the inherent performance limitations of software programmable systems mean that they are inadequate for high performance designs Designers thus turned to gate arrays as a solution User programmable gate arrays field programmable gate arrays FPGAs have recently emerged and are changing the way electronic systems are designed and implemented The growing complexity of the logic circuits that can be packed onto an FPGA chip means that it has become important to have automatic synthesis tools that implement logic functions on these architectures Logic Synthesis for Field Programmable Gate Arrays describes logic synthesis for both look up table LUT and multiplexor based architectures with a balanced presentation of existing techniques together with algorithms and the system developed by the authors Audience A useful reference for VLSI designers developers of computer aided design tools and anyone involved in or with FPGAs   **Logic Synthesis for Field Programmable Gate Arrays** Aiguo Lu,1995   <u>Logic Synthesis for Field-programmable Gate Arrays</u> Rajeev Murgai,1993   *Field-Programmable Gate Arrays* Stephen D. Brown,Robert J. Francis,Jonathan Rose,Zvonko G. Vranesic,2012-12-06 Field Programmable Gate Arrays FPGAs have emerged as an attractive means of implementing logic circuits providing instant manufacturing turnaround and negligible prototype costs They hold the promise of replacing much of the VLSI market now held by mask programmed gate arrays FPGAs offer an affordable solution for customized VLSI over a wide variety of applications and have also opened up new possibilities in designing reconfigurable digital systems Field Programmable Gate Arrays discusses the most important aspects of FPGAs in a textbook manner It provides the reader with a focused view of the key issues using a consistent notation and style of presentation It provides detailed descriptions of commercially available FPGAs and an in depth treatment of the FPGA architecture and CAD issues that are the subjects of current research The material presented is of interest to a variety of readers including those who are not familiar with FPGA technology but wish to be introduced to it as well as those who already have an understanding of FPGAs but who are interested in learning about the research directions that are of current interest   **Logic Synthesis for FPGA-Based Mealy Finite State Machines** Alexander Barkalov,Larysa Titarenko,Kazimierz Krzywicki,2024-12-04 This book is devoted to the logic synthesis of field programmable gate array FPGA based circuits of Mealy finite state machines FSM Three new methods of state assignment are proposed which allows obtaining FSM circuits required minimum amount of internal chip resources Logic Synthesis for FPGA Based Mealy Finite State Machines Structural Decomposition in Logic Design contains several original synthesis and optimization methods based on the structural decomposition of FPGA based FSM circuits developed by the authors To optimize FSM

circuits the authors introduce the use of three methods of state assignment twofold extended and composite These methods allow for the creation of two or three level architectures of FSM circuits The authors also demonstrate how the proposed methods FSM architectures and synthesis methods can replace known solutions based on either functional decomposition or classical methods of structural decomposition The authors also show how these architectures have regular systems of interconnections and demonstrate positive features compared to methods based on functional decomposition including producing circuits with fewer elements that are faster and consume less power than their counterparts The book includes experimental results proving the efficiency of the proposed solutions and compares the numbers in Look up Tables LUTs showing the performance maximum operating frequency and power consumption for various methods of state assignment The audience for this book is students researchers and engineers specializing in computer science engineering electronics and telecommunications It will be especially useful for engineers working within the scope of algorithms hardware based software accelerators and control units and systems based on the use of FPGAs **Logic Synthesis for FPGA-Based Finite State Machines** Alexander Barkalov,Larysa Titarenko,Malgorzata Kolopienczyk,Kamil Mielcarek,Grzegorz Bazydlo,2015-10-15 This book discusses control units represented by the model of a finite state machine FSM It contains various original methods and takes into account the peculiarities of field programmable gate arrays FPGA chips and a FSM model It shows that one of the peculiarities of FPGA chips is the existence of embedded memory blocks EMB The book is devoted to the solution of problems of logic synthesis and reduction of hardware amount in control units The book will be interesting and useful for researchers and PhD students in the area of Electrical Engineering and Computer Science as well as for designers of modern digital systems *Memory-Based Logic Synthesis* Tsutomu Sasao,2011-03-01 This book describes the synthesis of logic functions using memories It is useful to design field programmable gate arrays FPGAs that contain both small scale memories called look up tables LUTs and medium scale memories called embedded memories This is a valuable reference for both FPGA system designers and CAD tool developers concerned with logic synthesis for FPGAs

Improvements to Field-programmable Gate Array Design Efficiency Using Logic Synthesis Andrew C. Ling,2009 As Field Programmable Gate Array FPGA capacity can now support several processors on a single device the scalability of FPGA design tools and methods has emerged as a major obstacle for the wider use of FPGAs For example logic synthesis which has traditionally been the fastest step in the FPGA Computer Aided Design CAD flow now takes several hours to complete in a typical FPGA compile In this work we address this problem by focusing on two areas First we revisit FPGA logic synthesis and attempt to improve its scalability Specifically we look at a binary decision diagram BDD based logic synthesis flow referred to as FBDD where we improve its runtime by several fold with a marginal impact to the resulting circuit area We do so by speeding up the classical cut generation problem by an order of magnitude which enables its application directly at the logic synthesis level Following this we introduce a guided partitioning technique using a fast global budgeting formulation

which enables us to optimize individual pockets within the circuit without degrading the overall circuit performance By using partitioning we can significantly reduce the solution space of the logic synthesis problem and furthermore open up the possibility of parallelizing the logic synthesis step The second area we look at is the area of Engineering Change Orders ECOs ECOs are incremental modifications to a design late in the design flow This is beneficial since it is minimally disruptive to the existing circuit which preserves much of the engineering effort invested previously in the design In a design flow where most of the steps are fully automated ECOs still remain largely a manual process This can often tie up a designer for weeks leading to missed project deadlines which is very detrimental to products whose life cycle can span only a few months As a solution to this we show how we can leverage existing logic synthesis techniques to automatically modify a circuit in a minimally disruptive manner This can significantly reduce the turn around time when applying ECOs **Logic Synthesis for Lookup-table Based Field Programmable Gate Arrays** Yean-Yow Hwang,1999 **Improvements to Field-programmable Gate Array Design Efficiency Using Logic Synthesis** Andrew C. Ling,2009 As Field Programmable Gate Array FPGA capacity can now support several processors on a single device the scalability of FPGA design tools and methods has emerged as a major obstacle for the wider use of FPGAs For example logic synthesis which has traditionally been the fastest step in the FPGA Computer Aided Design CAD flow now takes several hours to complete in a typical FPGA compile In this work we address this problem by focusing on two areas First we revisit FPGA logic synthesis and attempt to improve its scalability Specifically we look at a binary decision diagram BDD based logic synthesis flow referred to as FBDD where we improve its runtime by several fold with a marginal impact to the resulting circuit area We do so by speeding up the classical cut generation problem by an order of magnitude which enables its application directly at the logic synthesis level Following this we introduce a guided partitioning technique using a fast global budgeting formulation which enables us to optimize individual pockets within the circuit without degrading the overall circuit performance By using partitioning we can significantly reduce the solution space of the logic synthesis problem and furthermore open up the possibility of parallelizing the logic synthesis step The second area we look at is the area of Engineering Change Orders ECOs ECOs are incremental modifications to a design late in the design flow This is beneficial since it is minimally disruptive to the existing circuit which preserves much of the engineering effort invested previously in the design In a design flow where most of the steps are fully automated ECOs still remain largely a manual process This can often tie up a designer for weeks leading to missed project deadlines which is very detrimental to products whose life cycle can span only a few months As a solution to this we show how we can leverage existing logic synthesis techniques to automatically modify a circuit in a minimally disruptive manner This can significantly reduce the turn around time when applying ECOs **Field-programmable Gate Array Logic Synthesis Using Boolean Satisfiability [microform]** Andrew C. Ling,2005 Field Programmable gate arrays FPGAs are reprogrammable logic chips that can be configured to implement various digital circuits FPGAs are fast replacing

custom ASICs in many areas due to their flexibility and fast turn around times for product development However these benefits come at a heavy cost of area speed and power The FPGA architecture and technology mapping phase are fundamental in determining the performance of the FPGA This thesis presents novel tools using Boolean satisfiability SAT to aid in both these areas First an architecture efficiency evaluation tool is developed The tool works by reading in a description of the FPGA architecture and rates how flexible that architecture can be in implementing various circuits Next a novel technology mapping approach is developed and compared to current methods This work contrasts with current approaches since it can be applied to almost any FPGA architecture Finally a resynthesis algorithm is described which rates the utility of current FPGA technology mappers where it can also be used to discover optimal configurations of common subcircuits to digital design   **Field-Programmable Gate Array Technology** Stephen M. Trimberger,Stephen Trimberger,1994-01-31 Many different kinds of FPGAs exist with different programming technologies different architectures and different software Field Programmable Gate Array Technology describes the major FPGA architectures available today covering the three programming technologies that are in use and the major architectures built on those programming technologies The reader is introduced to concepts relevant to the entire field of FPGAs using popular devices as examples Field Programmable Gate Array Technology includes discussions of FPGA integrated circuit manufacturing circuit design and logic design It describes the way logic and interconnect are implemented in various kinds of FPGAs It covers particular problems with design for FPGAs and future possibilities for new architectures and software This book compares CAD for FPGAs with CAD for traditional gate arrays It describes algorithms for placement routing and optimization of FPGAs Field Programmable Gate Array Technology describes all aspects of FPGA design and development For this reason it covers a significant amount of material Each section is clearly explained to readers who are assumed to have general technical expertise in digital design and design tools Potential developers of FPGAs will benefit primarily from the FPGA architecture and software discussion Electronics systems designers and ASIC users will find a background to different types of FPGAs and applications of their use   **Field-Programmable Logic: Architectures, Synthesis and Applications** Reiner W. Hartenstein,1994-08-24 This volume contains the proceedings of the 4th International Workshop on Field Programmable Logic and Applications FPL 94 held in Prague Czech Republic in September 1994 The growing importance of field programmable devices is substantiated by the remarkably high number of 116 submissions for FPL 94 from them the revised versions of 40 full papers and 24 high quality poster presentations were accepted for inclusion in this volume Among the topics treated are testing layout synthesis tools compilation research and CAD trade offs and experience innovations and smart applications FPGA based computer architectures high level design prototyping and ASIC emulators commercial devices new tools CCMs and HW SW co design modelers educational experience and novel architectures   *Field-Programmable Gate Array Technology* Stephen M. Trimberger,2012-12-06 Many different kinds of FPGAs exist with different programming technologies different architectures

and different software Field Programmable Gate Array Technology describes the major FPGA architectures available today covering the three programming technologies that are in use and the major architectures built on those programming technologies The reader is introduced to concepts relevant to the entire field of FPGAs using popular devices as examples Field Programmable Gate Array Technology includes discussions of FPGA integrated circuit manufacturing circuit design and logic design It describes the way logic and interconnect are implemented in various kinds of FPGAs It covers particular problems with design for FPGAs and future possibilities for new architectures and software This book compares CAD for FPGAs with CAD for traditional gate arrays It describes algorithms for placement routing and optimization of FPGAs Field Programmable Gate Array Technology describes all aspects of FPGA design and development For this reason it covers a significant amount of material Each section is clearly explained to readers who are assumed to have general technical expertise in digital design and design tools Potential developers of FPGAs will benefit primarily from the FPGA architecture and software discussion Electronics systems designers and ASIC users will find a background to different types of FPGAs and applications of their use   *Synthesis and Optimization of FPGA-Based Systems* Valery Sklyarov,Iouliia Skliarova,Alexander Barkalov,Larysa Titarenko,2014-03-14 The book is composed of two parts The first part introduces the concepts of the design of digital systems using contemporary field programmable gate arrays FPGAs Various design techniques are discussed and illustrated by examples The operation and effectiveness of these techniques is demonstrated through experiments that use relatively cheap prototyping boards that are widely available The book begins with easily understandable introductory sections continues with commonly used digital circuits and then gradually extends to more advanced topics The advanced topics include novel techniques where parallelism is applied extensively These techniques involve not only core reconfigurable logical elements but also use embedded blocks such as memories and digital signal processing slices and interactions with general purpose and application specific computing systems Fully synthesizable specifications are provided in a hardware description language VHDL and are ready to be tested and incorporated in engineering designs A number of practical applications are discussed from areas such as data processing and vector based computations e g Hamming weight counters comparators The second part of the book covers the more theoretical aspects of finite state machine synthesis with the main objective of reducing basic FPGA resources minimizing delays and achieving greater optimization of circuits and systems   **Logic Synthesis and Optimization** Tsutomu Sasao,2012-12-06 Logic Synthesis and Optimization presents up to date research information in a pedagogical form The authors are recognized as the leading experts on the subject The focus of the book is on logic minimization and includes such topics as two level minimization multi level minimization application of binary decision diagrams delay optimization asynchronous circuits spectral method for logic design field programmable gate array FPGA design EXOR logic synthesis and technology mapping Examples and illustrations are included so that each contribution can be read independently Logic Synthesis and Optimization is an indispensable reference

for academic researchers as well as professional CAD engineers   <u>Logic Synthesis for Finite State Machines Based on Linear Chains of States</u> Alexander Barkalov,Larysa Titarenko,Jacek Bieganowski,2017-06-24 This book discusses Moore finite state machines FSMs implemented with field programmable gate arrays FPGAs including look up table LUT elements and embedded memory blocks EMBs To minimize the number of LUTs in FSM logic circuits the authors propose replacing a state register with a state counter They also put forward an approach allowing linear chains of states to be created which simplifies the system of input memory functions and therefore decreases the number of LUTs in the resulting FSM circuit The authors combine this approach with using EMBs to implement the system of output functions microoperations This allows a significant decrease in the number of LUTs as well as eliminating a lot of interconnections in the FSM logic circuit As a rule it also reduces the area occupied by the circuit and diminishes the resulting power dissipation This book is an interesting and valuable resource for students and postgraduates in the area of computer science as well as for designers of digital systems that included complex control units   *Digital Signal Processing with Field Programmable Gate Arrays* Uwe Meyer-Baese,2007-09-28 A practical and fascinating book on a topic at the forefront of communications technology Field Programmable Gate Arrays FPGAs are on the verge of revolutionizing digital signal processing Novel FPGA families are replacing ASICs and PDSPs for front end digital signal processing algorithms at an accelerating rate The efficient implementation of these algorithms is the main goal of this book It starts with an overview of today s FPGA technology devices and tools for designing state of the art DSP systems Each of the book s chapter contains exercises The VERILOG source code and a glossary are given in the appendices   **Digital Design Using Field Programmable Gate Arrays** Pak K. Chan,Samiha Mourad,1994 For graduate and undergraduate students as well as professionals in the field of digital design This is the first book to offer a complete description of FPGAs and the methods involved in using CAD design tools for implementation of digital systems using FPGAs It covers both general concepts of systems and logic design and specific issues related to FPGAs themselves with reference to all existing technologies KEY TOPICS Provides a complete approach to digital systems specification synthesis implementation and prototyping Outlines all steps in using FPGA technology in logic design from description of the problem to realization and contains practical detailed examples throughout   **Digital Signal Processing with Field Programmable Gate Arrays** U. Meyer-Baese,2013-03-09 Field Programmable Gate Arrays FPGAs are on the verge of revolutionizing digital signal processing Novel FPGA families are replacing ASICs and PDSPs for front end digital signal processing algorithms more and more The efficient implementation of these algorithms is the main goal of this book It starts with an overview of today s FPGA technology devices and tools for designing state of the art DSP systems A case study in the first chapter is the basis for more than 30 design examples The following chapters deal with computer arithmetic concepts theory and the implementation of FIR and IIR filters multirate digital signal processing systems DFT and FFT algorithms and advanced algorithms with high future potential Each chapter contains exercises The VERILOG source

code and a glossary are given in the appendices The accompanying CD ROM contains the examples in VHDL and Verilog code as well as the newest Altera Baseline software 5 Stars this book is well written and covers many of the aspects of DSP with FPGAs I run a business that specializes exclusively in high performance DSP designs using FPGAs This book pretty much covers it all in fact it closely parallels the material we present in our DSP for FPGAs seminar I very highly recommend this book Ray Andraka of Andraka Consultants N Kingstown RI

This book delves into Logic Synthesis For Field Programmable Gate Arrays. Logic Synthesis For Field Programmable Gate Arrays is an essential topic that must be grasped by everyone, ranging from students and scholars to the general public. The book will furnish comprehensive and in-depth insights into Logic Synthesis For Field Programmable Gate Arrays, encompassing both the fundamentals and more intricate discussions.

1. This book is structured into several chapters, namely:

   - Chapter 1: Introduction to Logic Synthesis For Field Programmable Gate Arrays
   - Chapter 2: Essential Elements of Logic Synthesis For Field Programmable Gate Arrays
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   - Chapter 4: Logic Synthesis For Field Programmable Gate Arrays in Specific Contexts
   - Chapter 5: Conclusion

2. In chapter 1, this book will provide an overview of Logic Synthesis For Field Programmable Gate Arrays. The first chapter will explore what Logic Synthesis For Field Programmable Gate Arrays is, why Logic Synthesis For Field Programmable Gate Arrays is vital, and how to effectively learn about Logic Synthesis For Field Programmable Gate Arrays.
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4. In chapter 3, the author will examine the practical applications of Logic Synthesis For Field Programmable Gate Arrays in daily life. This chapter will showcase real-world examples of how Logic Synthesis For Field Programmable Gate Arrays can be effectively utilized in everyday scenarios.
5. In chapter 4, the author will scrutinize the relevance of Logic Synthesis For Field Programmable Gate Arrays in specific contexts. The fourth chapter will explore how Logic Synthesis For Field Programmable Gate Arrays is applied in specialized fields, such as education, business, and technology.
6. In chapter 5, the author will draw a conclusion about Logic Synthesis For Field Programmable Gate Arrays. The final chapter will summarize the key points that have been discussed throughout the book.
   This book is crafted in an easy-to-understand language and is complemented by engaging illustrations. It is highly recommended for anyone seeking to gain a comprehensive understanding of Logic Synthesis For Field Programmable Gate Arrays.

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Logic Synthesis For Field Programmable Gate Arrays Introduction

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adalah 154 cm² demikanlah pembahasan mengenai bagaimana cara menghitung luas bangun

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