Interconnect Analysis and Synthesis

Chung-Kuan Cheng John Lillis Shen Lin Norman Chang

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Kyung Hoae Koo

Interconnect Analysis And Synthesis:

Interconnect Analysis and Synthesis Chung-Kuan Cheng, 2000 State of the art methods and current perspectives on interconnect The irrepressible march toward smaller and faster integrated circuits has made interconnect a hot topic for semiconductor research The effects of wire size topology construction and network design on system performance and reliability have all been thoroughly investigated in recent years Interconnect Analysis and Synthesis provides CAD researchers and engineers with powerful state of the art tools for the analysis design and optimization of interconnect It brings together a wealth of information previously scattered throughout the literature explaining in depth available analysis techniques and presenting a range of CAD algorithms for synthesizing and optimizing interconnect Along with examples and results from the semiconductor industry and 150 illustrations this practical work features Models for interconnect as well as devices and the impact of scaling trends Modern analysis techniques from matrix reduction and moment matching to transmission line analysis An overview of the effects of inductance on on chip interconnect Flexible CAD algorithms that can be generalized for different needs from buffer insertion to wire sizing to routing topology Emphasis on realistic problem formulations addressing key design tradeoffs such as those between area and performance *Interconnect-Centric Design* for Advanced SOC and NOC Jari Nurmi, H. Tenhunen, J. Isoaho, Axel Jantsch, 2006-03-20 In Interconnect centric Design for Advanced SoC and NoC we have tried to create a comprehensive understanding about on chip interconnect characteristics design methodologies layered views on different abstraction levels and finally about applying the interconnect centric design in system on chip design Traditionally on chip communication design has been done using rather ad hoc and informal approaches that fail to meet some of the challenges posed by next generation SOC designs such as performance and throughput power and energy reliability predictability synchronization and management of concurrency To address these challenges it is critical to take a global view of the communication problem and decompose it along lines that make it more tractable We believe that a layered approach similar to that defined by the communication networks community should also be used for on chip communication design The design issues are handled on physical and circuit layer logic and architecture layer and from system design methodology and tools point of view Formal communication modeling and refinement is used to bridge the communication layers and network centric modeling of multiprocessor on chip networks and socket based design will serve the development of platforms for SoC and NoC integration Interconnect centric Design for Advanced SoC and NoC is concluded by two application examples interconnect and memory organization in SoCs for advanced set top boxes and TV and a case study in NoC platform design for more generic applications IC Interconnect Analysis Mustafa Celik, Larry Pileggi, Altan Odabasioglu, 2007-05-08 As integrated circuit IC feature sizes scaled below a quarter of a micron thereby defining the deep submicron DSM era there began a gradual shift in the impact on performance due to the metal interconnections among the active circuit components Once viewed as merely parasitics in terms of their relevance to the

overall circuit behavior the interconnect can now have a dominant impact on the IC area and performance Beginning in the late 1980 s there was significant research toward better modeling and characterization of the resistance capacitance and ultimately the inductance of on chip interconnect IC Interconnect Analysis covers the state of the art methods for modeling and analyzing IC interconnect based on the past fifteen years of research This is done at a level suitable for most practitioners who work in the semiconductor and electronic design automation fields but also includes significant depth for the research professionals who will ultimately extend this work into other areas and applications IC Interconnect Analysis begins with an in depth coverage of delay metrics including the ubiquitous Elmore delay and its many variations This is followed by an outline of moment matching methods calculating moments efficiently and Krylov subspace methods for model order reduction The final two chapters describe how to interface these reduced order models to circuit simulators and gate level timing analyzers respectively IC Interconnect Analysis is written for CAD tool developers IC designers and graduate students Symbolic Analysis and Reduction of VLSI Circuits Zhanhai Qin, Chung-Kuan Cheng, 2009-03-13 Symbolic analysis is an intriguing topic in VLSI designs The analysis methods are crucial for the applications to the parasitic reduction and analog circuit evaluation However analyzing circuits symbolically remains a challenging research issue Therefore in this book we survey the recent results as the progress of on going works rather than as the solution of the field For parasitic reduction we approximate a huge amount of electrical parameters into a simplified RLC network This reduction allows us to handle very large integrated circuits with given memory capacity and CPU time A symbolic analysis approach reduces the circuit according to the network topology Thus the designer can maintain the meaning of the original network and perform the analysis hierarchically For analog circuit designs symbolic analysis provides the relation between the tunable parameters and the characteristics of the circuit The analysis allows us to optimize the circuit behavior The book is divided into three parts Part I touches on the basics of circuit analysis in time domain and in s domain For an s domain expression the Taylor s expansion with s approaching infinity is equivalent to the time domain solution after the inverse Laplace transform On the other hand the Taylor's expansion when s approaches zero derives the moments of the output responses in time domain Part II focuses on the techniques for parasitic reduction In Chapter 2 we present the approximation methods to match the first few moments with reduced circuit orders In Chapter 3 we apply the Y Delta transformation to reduce the dynamic linear network The method finds the exact values of the low order coefficients of the numerator and denominator of the transfer function and thus matches part of the moments In Chapter 4 we handle two major issues of the Y Delta transformation common factors in fractional expressions and round off errors Chapter 5 explains the stability of the reduced expression in particular the Ruth Hurwitz Criterion We make an effort to describe the proof of the Criterion because the details are omitted in most of the contemporary textbooks In Chapter 6 we present techniques to synthesize circuits to approximate the reduced expressions after the transformation In Part III we discuss symbolic generation of the determinants and cofactors for

the application to analog designs In Chapter 7 we depict the classical topological analysis approach In Chapter 8 we describe a determinant decision diagram approach that exploits the sparsity of the matrix to accelerate the computation In Chapter 9 we take only significant terms when we search through determinant decision diagram to approximate the solution In Chapter 10 we extend the determinant decision diagram to a hierarchical model The construction of the modules through the hierarchy is similar to the Y Delta transformation in the sense that a byproduct of common factors appears in the numerator and denominator Therefore we describe the method to prune the common factors **The Comparison Study of Future** On-chip Interconnects for High Performance VLSI Applications Kyung Hoae Koo, 2011 Moore's law has driven the scaling of digital electronic devices dimensions and performances over the last 40 years As a result logic components in a microprocessor have shown dramatic performance improvement On the other hand an on chip interconnect which was considered only as a parasitic load before 1990s became the real performance bottleneck due to its extremely reduced cross section dimension Now on chip global interconnect with conventional Cu low k and delay optimized repeater scheme faces great challenges in the nanometer regime imposing problems of slower delay higher power dissipation and limited bandwidth Carbon based materials such as carbon nanotubes and graphene nanoribbons and optical interconnect have been proposed for the alternate solution for the future nodes due to their special physical characteristics. This dissertation investigates the basic physical properties of novel materials for future interconnect and describes the analytical and numerical models of local and global wire system based on new materials and novel signaling paradigms. This work also compares their basic performance metrics and circuit architectures to cope with the interconnect performance bottlenecks. We quantify the performance of these novel interconnects and compare them with Cu low k wires for future high performance ICs

On-Chip Communication Architectures Sudeep Pasricha, Nikil Dutt, 2010-07-28 Over the past decade system on chip SoC designs have evolved to address the ever increasing complexity of applications fueled by the era of digital convergence Improvements in process technology have effectively shrunk board level components so they can be integrated on a single chip New on chip communication architectures have been designed to support all inter component communication in a SoC design These communication architecture fabrics have a critical impact on the power consumption performance cost and design cycle time of modern SoC designs As application complexity strains the communication backbone of SoC designs academic and industrial R D efforts and dollars are increasingly focused on communication architecture design On Chip Communication Architectures is a comprehensive reference on concepts research and trends in on chip communication architecture design It will provide readers with a comprehensive survey not available elsewhere of all current standards for on chip communication architectures explaining key concepts surveying research efforts and predicting future trends Detailed analysis of all popular standards for on chip communication architectures Comprehensive survey of all research on communication architectures covering a wide range of topics relevant

to this area spanning the past several years and up to date with the most current research efforts Future trends that with have a significant impact on research and design of communication architectures over the next several years Methodology of Tree Microstrip Interconnects Modelling For Signal Distribution Blaise Ravelo, 2019-11-21 This book focuses on the modelling methodology of microstrip interconnects discussing various structures of single input multiple output SIMO tree interconnects for signal integrity SI engineering Further it describes lumped and distributed transmission line elements based on single input single output SIMO models of symmetric and asymmetric trees and investigates more complicated phenomenon such as interbranch coupling The modelling approaches are based on the analytical methods using the Z Y and T matrices The established method enables the S parameters and voltage transfer function of SIMO tree to be determined Providing illustrative results with frequency and time domain analyses for each tree interconnect structure the book is a valuable resource for researchers engineers and graduate students in fields of analogue RF microwave digital and mixed circuit design SI and manufacturing engineering Signal Integrity Effects in Custom IC and ASIC Designs Raminderpal Singh, 2001-12-12 offers a tutorial guide to IC designers who want to move to the next level of chip design by unlocking the secrets of signal integrity Jake Buurma Senior Vice President Worldwide Research Development Cadence Design Systems Inc Covers signal integrity effects in high performance Radio Frequency RF IC Brings together research papers from the past few years that address the broad range of issues faced by IC designers and CAD managers now and in the future A Wiley Advanced Model Order Reduction Techniques in VLSI Design Sheldon Tan, Lei He, 2007-05-31 **IEEE Press publication** Model order reduction MOR techniques reduce the complexity of VLSI designs paving the way to higher operating speeds and smaller feature sizes This book presents a systematic introduction to and treatment of the key MOR methods employed in general linear circuits using real world examples to illustrate the advantages and disadvantages of each algorithm Following a review of traditional projection based techniques coverage progresses to more advanced MOR methods for VLSI design including HMOR passive truncated balanced realization TBR methods efficient inductance modeling via the VPEC model and structure preserving MOR techniques Where possible numerical methods are approached from the CAD engineer s perspective avoiding complex mathematics and allowing the reader to take on real design problems and develop more effective tools With practical examples and over 100 illustrations this book is suitable for researchers and graduate students of electrical and computer engineering as well as practitioners working in the VLSI design industry (System-on-a-Chip) Testing for Plug and Play Test Automation Krishnendu Chakrabarty, 2002-09-30 Various aspects of system on a chip SOC integrated circuit testing are addressed in 13 papers on test planning access and scheduling test data compression and interconnect crosstalk and signal integrity Topics include concurrent test of core based SOC design and testing for interconnect crosstalk defects using on chip embedded processor cores The editor is affiliated with Duke University The book is reprinted from a Special Issue of the Journal of Electronic Testing vol 18 nos 4 5 There is no subject

index Annotation c 2003 Book News Inc Portland OR booknews com Low Power Interconnect Design Sandeep Saini, 2015-06-12 This book provides practical solutions for delay and power reduction for on chip interconnects and buses It provides an in depth description of the problem of signal delay and extra power consumption possible solutions for delay and glitch removal while considering the power reduction of the total system Coverage focuses on use of the Schmitt Trigger as an alternative approach to buffer insertion for delay and power reduction in VLSI interconnects In the last section of the book various bus coding techniques are discussed to minimize delay and power in address and data buses On-Chip Interconnects Ethiopia Enideg Nigussie, 2011-12-02 This book presents design techniques analysis and implementation of high performance and power efficient variation tolerant on chip interconnects Given the design paradigm shift to multi core interconnect centric designs and the increase in sources of variability and their impact in sub 100nm technologies this book will be an invaluable reference for anyone concerned with the design of next generation high performance electronics systems Proceedings of the European Computing Conference Nikos Mastorakis, Valeri Mladenov, Vassiliki T. Kontargyri, 2010-03-16 The European Computing Conference offers a unique forum for establishing new collaborations within present or upcoming research projects exchanging useful ideas presenting recent research results participating in discussions and establishing new academic collaborations linking university with the industry Engineers and Scientists working on various areas of Systems Theory Applied Mathematics Simulation Numerical and Computational Methods and Parallel Computing present the latest findings advances and current trends on a wide range of topics This proceedings volume will be of interest to students researchers and practicing engineers **Electronic Design Automation** for IC System Design, Verification, and Testing Luciano Lavagno, Igor L. Markov, Grant Martin, Louis K. Scheffer, 2017-12-19 The first of two volumes in the Electronic Design Automation for Integrated Circuits Handbook Second Edition Electronic Design Automation for IC System Design Verification and Testing thoroughly examines system level design microarchitectural design logic verification and testing Chapters contributed by leading experts authoritatively discuss processor modeling and design tools using performance metrics to select microprocessor cores for integrated circuit IC designs design and verification languages digital simulation hardware acceleration and emulation and much more New to This Edition Major updates appearing in the initial phases of the design flow where the level of abstraction keeps rising to support more functionality with lower non recurring engineering NRE costs Significant revisions reflected in the final phases of the design flow where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting edge applications and approaches realized in the decade since publication of the previous edition these are illustrated by new chapters on high level synthesis system on chip SoC block based design and back annotating system level models Offering improved depth and modernity Electronic Design Automation for IC System Design Verification and Testing provides a valuable state of the art reference for electronic design automation

EDA students researchers and professionals
Circuit Oriented Electromagnetic Modeling Using the PEEC Techniques Albert Ruehli, Giulio Antonini, Lijun Jiang, 2017-06-19 Bridges the gap between electromagnetics and circuits by addressing electrometric modeling EM using the Partial Element Equivalent Circuit PEEC method This book provides intuitive solutions to electromagnetic problems by using the Partial Element Equivalent Circuit PEEC method This book begins with an introduction to circuit analysis techniques laws and frequency and time domain analyses The authors also treat Maxwell s equations capacitance computations and inductance computations through the lens of the PEEC method Next readers learn to build PEEC models in various forms equivalent circuit models non orthogonal PEEC models skin effect models PEEC models for dielectrics incident and radiate field models and scattering PEEC models The book concludes by considering issues like stability and passivity and includes five appendices some with formulas for partial elements Leads readers to the solution of a multitude of practical problems in the areas of signal and power integrity and electromagnetic interference Contains fundamentals applications and examples of the PEEC method Includes detailed mathematical derivations Circuit Oriented Electromagnetic Modeling Using the PEEC Techniques is a reference for students researchers and developers who work on the physical layer modeling of IC interconnects and Packaging PCBs and high speed links

The VLSI Handbook Wai-Kai Chen, 2019-07-17 Over the years the fundamentals of VLSI technology have evolved to include a wide range of topics and a broad range of practices To encompass such a vast amount of knowledge The VLSI Handbook focuses on the key concepts models and equations that enable the electrical engineer to analyze design and predict the behavior of very large scale integrated circuits It provides the most up to date information on IC technology you can find Using frequent examples the Handbook stresses the fundamental theory behind professional applications Focusing not only on the traditional design methods it contains all relevant sources of information and tools to assist you in performing your job This includes software databases standards seminars conferences and more The VLSI Handbook answers all your needs in one comprehensive volume at a level that will enlighten and refresh the knowledge of experienced engineers and educate the novice This one source reference keeps you current on new techniques and procedures and serves as a review for standard practice It will be your first choice when looking for a solution **EDA for IC System Design, Verification,** and Testing Louis Scheffer, Luciano Lavagno, Grant Martin, 2018-10-03 Presenting a comprehensive overview of the design automation algorithms tools and methodologies used to design integrated circuits the Electronic Design Automation for Integrated Circuits Handbook is available in two volumes The first volume EDA for IC System Design Verification and Testing thoroughly examines system level design microarchitectural design logical verification and testing Chapters contributed by leading experts authoritatively discuss processor modeling and design tools using performance metrics to select microprocessor cores for IC designs design and verification languages digital simulation hardware acceleration and emulation and much more Save on the complete set **Dimension Reduction of Large-Scale Systems** Peter

Benner, Volker Mehrmann, Danny C. Sorensen, 2005-06-09 In the past decades model reduction has become an ubiquitous tool in analysis and simulation of dynamical systems control design circuit simulation structural dynamics CFD and many other disciplines dealing with complex physical models The aim of this book is to survey some of the most successful model reduction methods in tutorial style articles and to present benchmark problems from several application areas for testing and comparing existing and new algorithms As the discussed methods have often been developed in parallel in disconnected application areas the intention of the mini workshop in Oberwolfach and its proceedings is to make these ideas available to researchers and practitioners from all these different disciplines Handbook of Algorithms for Physical Design **Automation** Charles J. Alpert, Dinesh P. Mehta, Sachin S. Sapatnekar, 2008-11-12 The physical design flow of any project depends upon the size of the design the technology the number of designers the clock frequency and the time to do the design As technology advances and design styles change physical design flows are constantly reinvented as traditional phases are removed and new ones are added to accommodate changes in **Integrated Circuit and System Design** Enrico Macii, Vassilis Paliouras, Odysseas Koufopavlou, 2004-08-24 Welcometotheproceedings of PATMOS 2004 thefourteenthinaseries of int national workshops PATMOS 2004 was organized by the University of Patras with technical co sponsorship from the IEEE Circuits and Systems Society Over the years the PATMOS meeting has evolved into an important ropean event where industry and academia meet to discuss power and timing aspects in modern integrated circuit and system design PATMOS provides a forum for researchers to discuss and investigate the emerging challenges in sign methodologies and tools required to develop the upcoming generations of integrated circuits and systems We realized this vision this year by providing a technical program that contained state of the art technical contributions a keynote speech three invited talks and two embedded tutorials The technical program focused on timing performance and power consumption as well as architectural aspects with particular emphasis on modelling design charac rization analysis and optimization in the nanometer era This year a record 152 contributions were received to be considered for p sible presentation at PATMOS Despite the choice for an intense three day m ting only 51 lecture papers and 34 poster papers could be accommodated in the single track technical program The Technical Program Committee with the sistance of additional expert reviewers selected the 85 papers to be presented at PATMOS and organized them into 13 technical sessions As was the case with the PATMOS workshops the review process was anonymous full papers were required and several reviews were received per manuscript

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