# INTERACTION BETWEEN COMPILERS AND COMPUTER ARCHITECTURES

edited by:
Gyungho Lee
Pen-Chung Yew

# Interaction Between Compilers And Computer Architectures

**SA Dillow**

**Interaction Between Compilers And Computer Architectures:**

**Interaction Between Compilers and Computer Architectures** Gyungho Lee,Pen-Chung Yew,2013-03-14 Effective compilers allow for a more efficient execution of application programs for a given computer architecture while well conceived architectural features can support more effective compiler optimization techniques A well thought out strategy of trade offs between compilers and computer architectures is the key to the successful designing of highly efficient and effective computer systems From embedded micro controllers to large scale multiprocessor systems it is important to understand the interaction between compilers and computer architectures The goal of the Annual Workshop on Interaction between Compilers and Computer Architectures INTERACT is to promote new ideas and to present recent developments in compiler techniques and computer architectures that enhance each other s capabilities and performance Interaction Between Compilers and Computer Architectures is an updated and revised volume consisting of seven papers originally presented at the Fifth Workshop on Interaction between Compilers and Computer Architectures INTERACT 5 which was held in conjunction with the IEEE HPCA 7 in Monterrey Mexico in 2001 This volume explores recent developments and ideas for better integration of the interaction between compilers and computer architectures in designing modern processors and computer systems Interaction Between Compilers and Computer Architectures is suitable as a secondary text for a graduate level course and as a reference for researchers and practitioners in industry Interaction Between Compilers and Computer Architectures ,1997 Extended abstracts of the 20 presentations made at the Workshop INTERACT 2002 ,2002-01-01 This text presents information on architecture and parallel and high performance computing presented at the 6th Workshop on Interaction between Compilers and Computer Architecture INTERACT 2002 **2011 15th Workshop on Interaction Between Compilers and Computer Architectures** Workshop on Interaction between Compilers and Computer Architectures,2011 **Eighth Workshop on Interaction Between Compilers and Computer Architecture** ,2004-01-01 INTERACT 2004 presents new ideas and explores recent developments in compiler techniques and computer architectures that enhance each other s capabilities and performance Its papers cover various aspects of interaction between compilers and architectures in the design of high performance microprocessors embedded controllers multiprocessors and other parallel computer systems *The Interaction of Compilation Technology and Computer Architecture* David J. Lilja,Peter L. Bird,2012-12-06 In brief summary the following results were presented in this work A linear time approach was developed to find register requirements for any specified CS schedule or filled MRT An algorithm was developed for finding register requirements for any kernel that has a dependence graph that is acyclic and has no data reuse on machines with depth independent instruction templates We presented an efficient method of estimating register requirements as a function of pipeline depth We developed a technique for efficiently finding bounds on register require ments as a function of pipeline depth Presented experimental data to verify these new techniques discussed some interesting design points for register file

size on a number of different architectures REFERENCES 1 Robert P Colwell Robert P Nix John J O Donnell David B Papworth and Paul K Rodman A VLIW Architecture for a Trace Scheduling Com piler In Architectural Support for Programming Languages and Operating Systems pages 180 192 1982 2 C Eisenbeis W Jalby and A Lichnewsky Compile Time Optimization of Memory and Register Usage on the Cray 2 In Proceedings of the Second Workshop on Languages and Compilers Urbana l inois August 1989 3 C Eisenbeis William Jalby and Alain Lichnewsky Squeezing More CPU Performance Out of a Cray 2 by Vector Block Scheduling In Proceedings of Supercomputing 88 pages 237 246 1988 4 Michael J Flynn Very High Speed Computing Systems Proceedings of the IEEE 54 1901 1909 December 1966      **INTERACT-9 2005** Institute of Electrical and Electronics Engineers, Inc. Staff,Satvinder S Juss,2005-12-01 INTERACT 2005 looks to promote new ideas and presents recent developments in compiler techniques and computer architectures that enhance each other s capabilities and performance Its papers explore the many aspects of the interaction between compilers and architectures in the design of high performance microprocessors embedded controllers multiprocessors and other parallel computer systems      *Interaction Between Compilers and Computer Architectures, Annual Workshop on* ,      INTERACT-7 2003 ,2003      The Interaction of Compilation Technology and Computer Architecture David J. Lilja,Peter L. Bird,1994-05-31 In brief summary the following results were presented in this work A linear time approach was developed to find register requirements for any specified CS schedule or filled MRT An algorithm was developed for finding register requirements for any kernel that has a dependence graph that is acyclic and has no data reuse on machines with depth independent instruction templates We presented an efficient method of estimating register requirements as a function of pipeline depth We developed a technique for efficiently finding bounds on register require ments as a function of pipeline depth Presented experimental data to verify these new techniques discussed some interesting design points for register file size on a number of different architectures REFERENCES 1 Robert P Colwell Robert P Nix John J O Donnell David B Papworth and Paul K Rodman A VLIW Architecture for a Trace Scheduling Com piler In Architectural Support for Programming Languages and Operating Systems pages 180 192 1982 2 C Eisenbeis W Jalby and A Lichnewsky Compile Time Optimization of Memory and Register Usage on the Cray 2 In Proceedings of the Second Workshop on Languages and Compilers Urbana l inois August 1989 3 C Eisenbeis William Jalby and Alain Lichnewsky Squeezing More CPU Performance Out of a Cray 2 by Vector Block Scheduling In Proceedings of Supercomputing 88 pages 237 246 1988 4 Michael J Flynn Very High Speed Computing Systems Proceedings of the IEEE 54 1901 1909 December 1966      *2012 16th Workshop on Interaction Between Compilers and Computer Architectures (INTERACT 2012)* ,2012      **2012 16th Workshop on Interaction Between Compilers and Computer Architectures** IEEE Staff,2012-02-25      **Sixth Annual Workshop on Interaction Between Compilers and Computer Architectures** ,2002      Special Issue on Interaction Between Compilers and Computer Architectures Alex K. Jones,Gayatri Mehta,Xin Yuan,2012      **Proceedings, 9th Annual Workshop on Interaction Between Compilers and Computer Architectures**

,2005    **INTERACT** ,     Workshop on Interaction Between Compilers and Computer Architecture ,     **13th Workshop on Interaction Between Compilers and Computer Architectures 2009, (INTERACT-13)** University Department of Computer Science,2011     2011 15th Workshop on Interaction Between Compilers and Computer Architectures IEEE Staff,2011-02-12     Proceedings, 2011 15th Workshop on Interaction Between Compilers and Computer Architecture ,2011

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