



Guest Editors' Introduction

HOT INTERCONNECTS 12

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..... Hot Interconnects is an annual conference that specializes in state-of-the-art hardware and software architectures, and implementations of interconnection networks of all scales, ranging from on-chip, processor-memory interconnects to wide-area networks. It is the event where the high-performance computing and high-speed networking communities meet, and has a wide attendance both from industry and academia. Hot Interconnects 12 convened from 25 to 27 August 2004 at Stanford University; it included two days of paper sessions and one day of tutorials. Sponsored by the IEEE Computer Society Technical Committee on Microprocessors and Microcomputers, Hot Interconnects also has technical cosponsorship from the IEEE Communications Society Technical Committees on High-Speed Networking and Communications Switching and Routing.

In his keynote address, Nick McKeown of Stanford University argued that the industry should revisit some fundamental assumptions about the buffer sizes used in TCP/IP networks. In another keynote, Jonathan Turner of Washington University in St. Louis spoke about a motivation and strategy for network virtualization.

Researchers presented 15 papers; we select-

ed the articles included in this issue of *IEEE Micro* on the basis of the highest reviewer ratings, feedback from conference participants, and an overall match with the *IEEE Micro* profile.

The first article focuses on intersystem interconnects. Krishnan and Mayhew address the topic of congestion control in advanced switching interconnects (ASI). The ASI architecture is based on PCI Express and shares the same physical and link layers, but it provides additional capabilities for multiprocessing and peer-to-peer computing. This article introduces and evaluates a localized congestion control mechanism for such systems. PCI Express is also the focus of a second article by Liu et al., which evaluates the performance of Infiniband host communication adapters with PCI Express. Results indicate that PCI Express brings significant performance improvements over that of PCI X, both in terms of throughput and latency.

A second set of articles focuses on interconnects for large-scale multiprocessors. Dunning et al. evaluate the performance of the Cray XT's distributed shared-memory architecture through extensive benchmarking simulations. Results indicate that this interconnect's high bandwidth and low latency significantly

Hot Interconnects Proceedings

**Jose Duato, Sudhakar
Yalamanchili, Lionel Ni**



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Hot Interconnects : Proceedings ,2002 **9th Symposium on Hot Interconnects: Symposium on High Performance Interconnects: Proceedings on High Performance Interconnects 2001: Stanford, CA.** IEEE Computer Society, Technical Committee on Microprocesses and Microcomputers,2001 Hot Interconnects ,2007 **Hot Interconnects ,2001** 14th Symposium on High-Performance Interconnects ,2006 14th IEEE Symposium on High-Performance Interconnects ,2006-01-01 Hot Interconnects is an international forum where the high performance computing and high speed networking communities meet Researchers architects and designers from academia and industry explore new and emerging technologies in wired optical and wireless networking packet processing switching and routing HOTI 2006 spans the range from packet oriented chip to chip communication processor interconnects in computing clusters system area and storage networks through more traditional LANs MANs and WANs Hot Interconnects ,2007 *Hot Interconnects ,2003* **13th Symposium on High Performance Interconnects ,2005** *HOT Interconnects ,2005*

Correct Models of Parallel Computing S. Noguchi,Ota Masahiro,1997 The 21st century will be the age of network computing Among the many key technologies in this field parallel computing and networking technology will play very important roles In this book emphasis is placed on networking and modeling parallel computing The topics cover parallel computing algorithms parallel software massively parallel computing systems and related applications Articles cover parallel computing networking and related applications to initiate discussions Since the appearance of Transputer chip T9000 C104 and standardizations of IEEE1355 Transputer systems seem to have opened a new interesting area of parallel computing networking and many practical applications **Interconnection Networks** Jose Duato,Sudhakar Yalamanchili,Lionel Ni,2003 Foreword Foreword to the First Printing Preface Chapter 1 Introduction Chapter 2 Message Switching Layer Chapter 3 Deadlock Livelock and Starvation Chapter 4 Routing Algorithms Chapter 5 CollectiveCommunicationSupport Chapter 6 Fault Tolerant Routing Chapter 7 Network Architectures Chapter 8 Messaging Layer Software Chapter 9 Performance Evaluation Appendix A Formal Definitions for Deadlock Avoidance Appendix B Acronyms References Index

On-Chip Networks Natalie Enright,Li-shiuan Peh,2022-11-10 With the ability to integrate a large number of cores on a single chip research into on chip networks to facilitate communication becomes increasingly important On chip networks seek to provide a scalable and high bandwidth communication substrate for multi core and many core architectures High bandwidth and low latency within the on chip network must be achieved while fitting within tight area and power budgets In this lecture we examine various fundamental aspects of on chip network design and provide the reader with an overview of the current state of the art research in this field Table of Contents Introduction Interface with System Architecture Topology Routing Flow Control Router Microarchitecture Conclusions Error Control for Network-on-Chip Links Bo Fu,Paul Ampadu,2011-10-09 This book provides readers with a comprehensive review of the state of the art in error control for

Network on Chip NOC links Coverage includes detailed description of key issues in NOC error control faced by circuit and system designers as well as practical error control techniques to minimize the impact of these errors on system performance

Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology Luciano Lavagno,Igor L. Markov,Grant Martin,Louis K. Scheffer,2017-02-03 The second of two volumes in the Electronic Design Automation for Integrated Circuits Handbook Second Edition Electronic Design Automation for IC Implementation Circuit Design and Process Technology thoroughly examines real time logic RTL to GDSII a file format used to transfer data of semiconductor physical layout design flow analog mixed signal design physical verification and technology computer aided design TCAD Chapters contributed by leading experts authoritatively discuss design for manufacturability DFM at the nanoscale power supply network design and analysis design modeling and much more New to This Edition Major updates appearing in the initial phases of the design flow where the level of abstraction keeps rising to support more functionality with lower non recurring engineering NRE costs Significant revisions reflected in the final phases of the design flow where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting edge applications and approaches realized in the decade since publication of the previous edition these are illustrated by new chapters on 3D circuit integration and clock design Offering improved depth and modernity Electronic Design Automation for IC Implementation Circuit Design and Process Technology provides a valuable state of the art reference for electronic design automation EDA students researchers and professionals

Deadlock Resolution in Computer-Integrated Systems MengChu Zhou,Maria Pia Fanti,2018-10-08 Complex computer integrated systems offer enormous benefits across a wide array of applications including automated production transportation concurrent software and computer operating systems computer networks distributed database systems and many other automated systems Yet as these systems become more complex automated distributed and computing intensive the opportunity for deadlock issues rises exponentially Deadlock modeling detection avoidance and recovery are critical to improving system performance Deadlock Resolution in Computer Integrated Systems is the first text to summarize and comprehensively treat this issue in a systematic manner Consisting of contributions from prominent researchers in the field this book addresses deadlock free models and scheduling detection and recovery methods the formulation of dynamic control policies and comparison and industrial benchmark studies that evaluate various approaches The editors lay the foundation for exploring deadlock issues with a typical example of an automated manufacturing process illustrating three primary modeling methods digraphs Petri nets and automata and comparing their respective advantages and disadvantages Providing all of the important models and resolution approaches this book is the complete guide for electrical and control engineers and manufacturing intelligent and network systems designers to prevent and manage deadlock issues in their systems

Silicon Photonics III Lorenzo Pavesi,David J. Lockwood,2016-01-08 This book is volume III of a series of books on silicon photonics It reports on the

development of fully integrated systems where many different photonics component are integrated together to build complex circuits This is the demonstration of the fully potentiality of silicon photonics It contains a number of chapters written by engineers and scientists of the main companies research centers and universities active in the field It can be of use for all those persons interested to know the potentialities and the recent applications of silicon photonics both in microelectronics telecommunication and consumer electronics market High Performance Computing Systems and Applications Nikitas J. Dimopoulos, Kin F. Li, 2002 High Performance Computing Systems and Applications contains a selection of fully refereed papers presented at the 14th International Conference on High Performance Computing Systems and Applications held in Victoria Canada in June 2000 This book presents the latest research in HPC Systems and Applications including distributed systems and architecture numerical methods and simulation network algorithms and protocols computer architecture distributed memory and parallel algorithms It also covers such topics as applications in astrophysics and space physics cluster computing numerical simulations for fluid dynamics electromagnetics and crystal growth networks and the Grid and biology and Monte Carlo techniques High Performance Computing Systems and Applications is suitable as a secondary text for graduate level courses and as a reference for researchers and practitioners in industry **Design Technologies for Green and Sustainable Computing Systems** Partha Pratim Pande, Amlan Ganguly, Krishnendu Chakrabarty, 2013-07-17 This book provides a comprehensive guide to the design of sustainable and green computing systems GSC Coverage includes important breakthroughs in various aspects of GSC including multi core architectures interconnection technology data centers high performance computing HPC and sensor networks The authors address the challenges of power efficiency and sustainability in various contexts including system design computer architecture programming languages compilers and networking *Advances in Informatics* Dimitrios I. Fotiadis, Stavros D. Nikolopoulos, 2000 This volume addresses the state of the art and future directions of informatics Several senior researchers and graduate students present their research and work here The purpose of the book is to disseminate the latest scientific engineering and technical information in various fields of informatics It covers a wide range of subjects from theoretical computer science software engineering systems and scientific computing to networking and applied research The book can be used either as a reference for related scientific work or as educational material for advanced computer science courses

Reviewing **Hot Interconnects Proceedings**: Unlocking the Spellbinding Force of Linguistics

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