

## THE IMPLEMENTATION AND APPLICATION OF MICRO ROLLBACK IN FAULT-TOLERANT VLSI SYSTEMS†

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### ABSTRACT

Concurrent error detection and confinement requires checking the outputs of every module in the system during every clock cycle. This is usually accomplished by checkers and isolation circuits in the communication paths from each module to the rest of the system. This additional circuitry reduces system performance. We present a technique, called *micro rollback*, which allows most of the performance penalty for concurrent error detection to be eliminated. Detection is performed in *parallel* with the transmission of information between modules, thus removing the delay for detection from the critical path. Erroneous information may thus reach its destination module several clock cycles before an error indication. Operations performed on this erroneous information are "undone" using a hardware mechanism for fast rollback of a few cycles. We discuss the implementation of a VLSI processor capable of micro rollback as well as several critical issues related to its use in a complete system.

### 1. Introduction

One of the keys to achieving a high degree of fault tolerance is the ability to detect errors immediately after they occur and prevent erroneous information from spreading throughout the system. In order to achieve concurrent error detection and confine the damage caused by the error to the failed module, it is often necessary to check the outputs of the module during every clock cycle. These requirements are usually satisfied by connecting checkers and isolation circuits in the communication path from each module to the rest of the system. As a result, either the clock cycle time must be increased to allow the checks to complete or additional pipeline stages are added to the system, thus slowing down the system whenever the pipeline needs to be flushed or is not full due to data dependencies. Hence, systems with high-coverage concurrent error detection often experience significant performance penalties due to checking delays. This problem is especially important in VLSI implementations, where checkers often contain many series stages, and may introduce as much or more delay than the circuit being checked. These delays can compound as, for example, when a processor reads a memory word, and (1) Hamming Code checks are made, (2) the word is encoded for bus transmission, and (3) the word is checked when it arrives at the processor before use.

One way to solve the problem described above is to perform checking in *parallel* with the transmission of information between modules. The receiving module does not wait for checks to complete. It proceeds with execution as the check is being carried out and the checking result is sent one (or a few) cycles later.

Performing error checking in parallel with inter-module communication largely solves the problem of checking delays, but it introduces a new problem in recovery. The state of the system (starting with the receiving module) may be polluted with damaged information before an error signal arrives. Therefore it is necessary to back up processing to the state that existed just before the error first occurred. This returns the system to an error-free state where the offending operation can be retried (or correction may be attempted by other means such as restoring information from a redundant module or initiating higher level rollback). We call the process of backing up a system several cycles in response to a delayed error signal *micro rollback*. In order to support micro rollback, each module in the system must buffer all the information necessary to undo the state changes that have occurred in the last few cycles.

Micro-rollback differs from single-instruction retry [2] in that it occurs at a lower level - on the basis of clock cycles rather than instructions. Since the system undoes cycles rather than instructions, it can be done at the logic level without keeping track of microprogram-level instruction semantics and instruction pipeline conditions. As a result, the micro rollback capability can be independently implemented in each module of a synchronous system following very simple specifications. Moreover, our work is specifically aimed at efficient VLSI implementation techniques for supporting micro rollback.

This paper discusses the micro architecture and VLSI implementation of a VLSI RISC processor that is capable of micro rollback. We show how the updated state of the entire processor can be checkpointed after every cycle without replicating all the storage. The VLSI implementation of the basic building blocks needed for micro rollback is discussed. It is shown that the micro rollback functionality can be added with only a small performance penalty and with a low area penalty relative to the size of the entire chip. We show how the concept of micro rollback can be used throughout the system, discuss the requirements from modules other than the processor, and show how the various modules operate in a multiprocessor system.

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**International Symposium on Fault-Tolerant Computing, 18th, 1988 (FTCS-18): Digest of Papers**, 1988

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NASA SP-7500 United States. National Aeronautics and Space Administration, **Proceedings of the 1995**

**International Conference on Parallel Processing** Prithviraj Banerjee, 1995-08-08 This set of technical books contains all the information presented at the 1995 International Conference on Parallel Processing This conference held August 14 18 featured over 100 lectures from more than 300 contributors and included three panel sessions and three keynote addresses The international authorship includes experts from around the globe from Texas to Tokyo from Leiden to London Compiled by faculty at the University of Illinois and sponsored by Penn State University these Proceedings are a comprehensive look at all that s new in the field of parallel processing *Management*, 1990 *On-Line Testing for VLSI* Michael Nicolaidis, Yervant Zorian, Dhiraj Pradhan, 2013-03-09 Test functions fault detection diagnosis error correction repair etc that are applied concurrently while the system continues its intended function are defined as on line testing In its expanded scope on line testing includes the design of concurrent error checking subsystems that can be themselves self checking fail safe systems that continue to function correctly even after an error occurs reliability monitoring and self test and fault tolerant designs On Line Testing for VLSI contains a selected set of articles that discuss many of the modern aspects of on line testing as faced today The contributions are largely derived from recent IEEE International On Line Testing Workshops Guest editors Michael Nicolaidis Yervant Zorian and Dhiraj Pradhan organized the articles into six chapters In the first chapter the editors introduce a large number of approaches with an expanded bibliography in which some references date back to the sixties On Line Testing for VLSI is an edited volume of original research comprising invited contributions by leading researchers **Management, a Bibliography for NASA Managers**, 1989 Software Design for Resilient Computer Systems Igor Schagaev, Jürg Gutknecht, 2024-07-15 This book addresses the question of how system software should be designed to account for faults and which fault tolerance features should provide for highest reliability With this third edition of *Software Design for Resilient Computer Systems* the book is thoroughly updated to contain the newest advice regarding software resilience With a new introductory chapter the new edition is ideal for researchers and industry professionals In the book the authors first show how system software interacts with the hardware to tolerate faults They analyze and further develop the theory of fault tolerance to understand the diverse ways to increase the reliability of a system with special attention on the role of system software in this process They introduce the theory of redundancy and its use for construction of a subsystem through generalised algorithm of fault tolerance GAFT and apply it to distributed systems The book s approach is applied to various hardware subsystems different structures of RAM and processor cores and demonstrates exceptional performance reliability and energy efficiency This third edition devotes substantial attention to system software

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*Fault Tolerance* Peter A. Lee,Thomas Anderson,2012-12-06 The production of a new version of any book is a daunting task as many authors will recognise In the field of computer science the task is made even more daunting by the speed with which the subject and its supporting technology move forward Since the publication of the first edition of this book in 1981 much research has been conducted and many papers have been written on the subject of fault tolerance Our aim then was to present for the first time the principles of fault tolerance together with current practice to illustrate those principles We believe that the principles have so far stood the test of time and are as appropriate today as they were in 1981 Much work on the practical applications of fault tolerance has been undertaken and techniques have been developed for ever more complex situations such as those required for distributed systems Nevertheless the basic principles remain the same

**Distributed Applications and Interoperable Systems** Twittie Senivongse,Rui Oliveira,2009-06-04 This book constitutes the refereed proceedings of the 9th IFIP WG 6.1 International Conference on Distributed Applications and Interoperable Systems DAIS 2009 held in Lisbon Portugal in June 2009 The DAIS conference was held as part of the federated event on Distributed Computing Techniques DisCoTec together with the 11th International Conference on Coordination Models and Languages Coordination 2009 and the IFIP WG 6.1 International Conference on Formal Techniques for Distributed Systems FMOODS FORTE 2009 The 12 revised full papers presented were carefully reviewed and selected from 32 submissions The papers address service orientation quality of service and service contract business processes Web

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**Proceedings, the IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems, November 13-15, 1995, Lafayette, Louisiana** IEEE Computer Society,1995 An invited talk recounts Intel s experience with increasing die yield through CAD algorithms and a panel discussion examines tools for the extracting of critical areas for a yield analysis of VLSI design Others of the 34 papers cover critical area analysis defect sensitivity and reliability fault tolerant architectures and arrays yield projection and enhancement fault tolerant and testing techniques and self checking and coding techniques No subject index Annotation copyright by Book News Inc Portland OR

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Electrical & Electronics Abstracts ,1988

**Dependable Systems: Software, Computing, Networks** Jürg Kohlas,Bertrand Meyer,André Schiper,2006-07-31 Modern civilization relies on a functioning information infrastructure As a result dependability has become a central issue in all disciplines of systems engineering and software architecture Theories methods and tools that help to master the problems encountered in the design process and the management of operations are therefore of utmost importance for the future of information and communication technology The present volume documents the results of a research program on Dependable Information and Communication Systems DICS The members of the project met in two workshops organized by the Hasler Foundation This state of the art survey contains 3 overview articles identifying major issues of dependability and presenting the latest solutions as well as 10 carefully selected and revised papers depicting the research results originating from those workshops The first workshop took place in Münchenwiler Switzerland in March 2004 and the second workshop which marked the conclusion of the projects in Lwenberg Switzerland in October 2005 The papers are organized in topical sections on surveys dependable software dependable computing and dependable networks

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drawn mainly from the annual International Conferences on Applications and Theory of Petri Nets Selected papers from the latest conference are independently refereed and revised and extended as necessary Some further papers submitted directly to the editor are included Advances in Petri Nets 1991 covers the 11th International Conference on Applications and Theory of Petri Nets held in Paris France in June 1991 The volume contains the Bibliography of Petri Nets 1990 prepared by H Pl  
nnecke and W Reisig with over 4000 entries PUBLISHER S WEBSITE **Proceedings** Symposium on Reliable Distributed Systems 14, 1995, Bad Neuenahr,1995 Search Based Software Engineering Günther Ruhe,Yuanyuan Zhang,2013-08-16 This book constitutes the refereed proceedings of the Fifth International Symposium on Search Based Software Engineering SSBSE 2013 held in St Petersburg Russia The 14 revised full papers 6 revised short papers and 6 papers of the graduate track presented together with 2 keynotes 2 challenge track papers and 1 tutorial paper were carefully reviewed and selected from 50 initial submissions Search Based Software Engineering SBSE studies the application of meta heuristic optimization techniques to various software engineering problems ranging from requirements engineering to software testing and maintenance

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