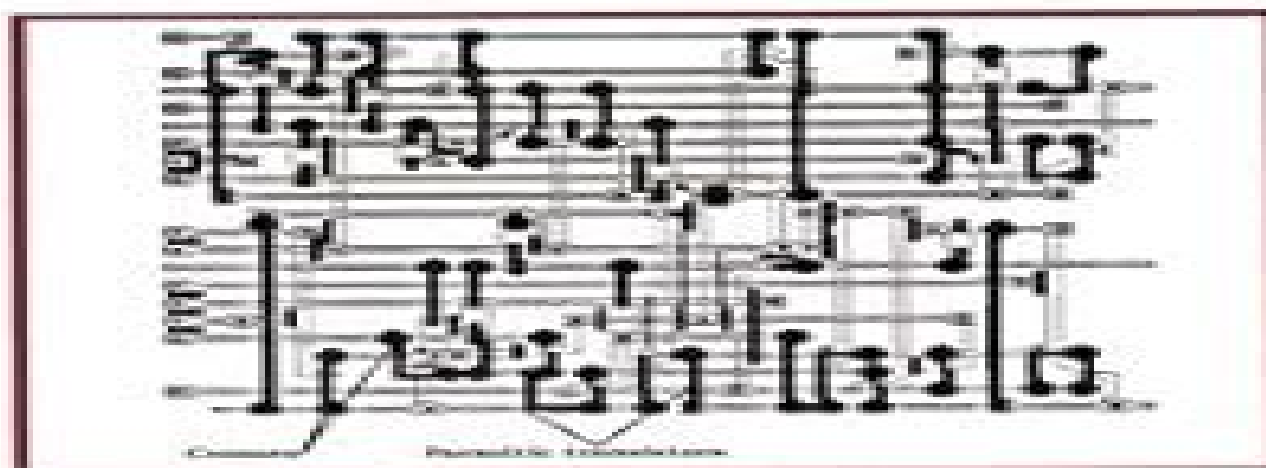


# INTEGRATED CIRCUIT DEFECT-SENSITIVITY:

## THEORY AND COMPUTATIONAL MODELS

José Pineda de Gyvez



Kluwer Academic Publishers

# Integrated Circuit Defect Sensitivity Theory And Computational Models

**D Kirk**

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## **Integrated Circuit Defect Sensitivity Theory And Computational Models:**

**Integrated Circuit Defect-Sensitivity: Theory and Computational Models** Jose Pineda de Gyvez,1992-12-31 The history of this book begins way back in 1982 At that time a research proposal was filed with the Dutch Foundation for Fundamental Research on Matter concerning research to model defects in the layer structure of integrated circuits It was projected that the results may be useful for yield estimates fault statistics and for the design of fault tolerant structures The reviewers were not in favor of this proposal and it disappeared in the drawers Shortly afterwards some microelectronics industries realized that their survival may depend on a better integration between technology and design laboratories For years the silicon foundry concept had suggested a fairly rigorous separation between the two areas The expectation was that many small design companies would share the investment into the extremely costly Silicon fabrication plants while designing large lots of application specific integrated circuits ASIC s Those fabrication plants would be concentrated with only a few market leaders     *Integrated Circuit Defect-Sensitivity* Jose Pineda De Gyvez,2014-09-01     **Integrated Circuit Defect-Sensitivity: Theory and Computational Models** José Pineda de Gyvez,2013-11-27 The history of this book begins way back in 1982 At that time a research proposal was filed with the Dutch Foundation for Fundamental Research on Matter concerning research to model defects in the layer structure of integrated circuits It was projected that the results may be useful for yield estimates fault statistics and for the design of fault tolerant structures The reviewers were not in favor of this proposal and it disappeared in the drawers Shortly afterwards some microelectronics industries realized that their survival may depend on a better integration between technology and design laboratories For years the silicon foundry concept had suggested a fairly rigorous separation between the two areas The expectation was that many small design companies would share the investment into the extremely costly Silicon fabrication plants while designing large lots of application specific integrated circuits ASIC s Those fabrication plants would be concentrated with only a few market leaders     *Scientific and Technical Aerospace Reports* ,1994     Chip On Board John H. Lau,1994-06-30 This book is a one stop guide to the state of the art of COB technology For professionals active in COB and MCM research and development those who wish to master COB and MCM problem solving methods and those who must choose a cost effective design and high yield manufacturing process for their interconnect systems here is a timely summary of progress in al aspects of this fascinating field It meets the reference needs of design material process equipment manufacturing quality reliability packaging and system engineers and technical managers working in electronic packaging and interconnection     **Proceedings, the IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems, November 13-15, 1995, Lafayette, Louisiana** IEEE Computer Society,1995 An invited talk recounts Intel s experience with increasing die yield through CAD algorithms and a panel discussion examines tools for the extracting of critical areas for a yield analysis of VLSI design Others of the 34 papers cover critical area analysis defect sensitivity and reliability fault tolerant architectures and arrays yield projection and

enhancement fault tolerant and testing techniques and self checking and coding techniques No subject index Annotation copyright by Book News Inc Portland OR *Integrated Circuit Manufacturability* José Pineda de Gyvez, Dhiraj Pradhan, 1998-10-30 INTEGRATED CIRCUIT MANUFACTURABILITY provides comprehensive coverage of the process and design variables that determine the ease and feasibility of fabrication or manufacturability of contemporary VLSI systems and circuits This book progresses from semiconductor processing to electrical design to system architecture The material provides a theoretical background as well as case studies examining the entire design for the manufacturing path from circuit to silicon Each chapter includes tutorial and practical applications coverage INTEGRATED CIRCUIT MANUFACTURABILITY illustrates the implications of manufacturability at every level of abstraction including the effects of defects on the layout their mapping to electrical faults and the corresponding approaches to detect such faults The reader will be introduced to key practical issues normally applied in industry and usually required by quality product and design engineering departments in today's design practices Yield management strategies Effects of spot defects Inductive fault analysis and testing Fault tolerant architectures and MCM testing strategies This book will serve design and product engineers both from academia and industry It can also be used as a reference or textbook for introductory graduate level courses on manufacturing *Bibliographic Index*, 1995 *IEEE/SEMI International Semiconductor Manufacturing Science Symposium* IEEE/SEMI International Semiconductor Manufacturing Science Symposium, 1993 Great Lakes 4th Symposium on VLSI IEEE, 1994 The proceedings of GSLV 94 held at the U of Notre Dame South Bend Indiana in March 1994 comprise technical papers in sessions on high level synthesis and verification systolic arrays fault tolerance theoretical results in routing logic synthesis MCM high performance architectures application specific design routing algorithms circuit

**IC defect-sensitivity** José de Jesús Pineda de Gyvez, 1991 **From Contamination to Defects, Faults and Yield Loss** Jitendra B. Khare, Wojciech Maly, 2012-12-06 Over the years there has been a large increase in the functionality available on a single integrated circuit This has been mainly achieved by a continuous drive towards smaller feature sizes larger dies and better packing efficiency However this greater functionality has also resulted in substantial increases in the capital investment needed to build fabrication facilities Given such a high level of investment it is critical for IC manufacturers to reduce manufacturing costs and get a better return on their investment The most obvious method of reducing the manufacturing cost per die is to improve manufacturing yield Modern VLSI research and engineering which includes design manufacturing and testing encompasses a very broad range of disciplines such as chemistry physics material science circuit design mathematics and computer science Due to this diversity the VLSI arena has become fractured into a number of separate sub domains with little or no interaction between them This is the case with the relationships between testing and manufacturing From Contamination to Defects Faults and Yield Loss Simulation and Applications focuses on the core of the interface between manufacturing and testing i e the contamination defect fault relationship The understanding of

this relationship can lead to better solutions of many manufacturing and testing problems Failure mechanism models are developed and presented which can be used to accurately estimate probability of different failures for a given IC This information is critical in solving key yield related applications such as failure analysis fault modeling and design manufacturing

**IC Defect-sensitivity** José Jesús de Pineda de Gyvez, 1991 The Science and Engineering of Microelectronic Fabrication Stephen A. Campbell, 1996 The Science and Engineering of Microelectronic Fabrication provides an introduction to microelectronic processing Geared towards a wide audience it may be used as a textbook for both first year graduate and upper level undergraduate courses and as a handy reference for professionals The text covers all the basic unit processes used to fabricate integrated circuits including photolithography plasma and reactive ion etching ion implantation diffusion oxidation evaporation vapor phase epitaxial growth sputtering and chemical vapor deposition Advanced processing topics such as rapid thermal processing nonoptical lithography molecular beam epitaxy and metal organic chemical vapor deposition are also presented The physics and chemistry of each process is introduced along with descriptions of the equipment used for the manufacturing of integrated circuits The text also discusses the integration of these processes into common technologies such as CMOS double poly bipolar and GaAs MESFETs Complexity performance tradeoffs are evaluated along with a description of the current state of the art devices Each chapter includes sample problems with solutions The book also makes use of the process simulation package SUPREM to demonstrate impurity profiles of practical interest *Forthcoming Books* Rose Arny, 1993-04 American Book Publishing Record ,1992 *Flip Chip Technologies* John H. Lau, 1996 A guide to flip chip technologies for professionals in flip chip and MCM research and development and for engineers and technical managers choosing design and manufacturing processes for electronic packaging and interconnect systems Discusses economic design material quality and reliability issues of flip chip technologies and details aspects of classical solder bumped flip chip interconnect technologies the next generations of flip chip technologies and known good die testing for multiple module applications Annotation copyright by Book News Inc Portland OR Government Reports Annual Index , Sections 1 2 Keyword Index Section 3 Personal author index Section 4 Corporate author index Section 5 Contract grant number index NTIS order report number index 1 E Section 6 NTIS order report number index F Z Electronics Manufacturing : with Lead-Free, Halogen-Free, and Conductive-Adhesive Materials John Lau, C.P. Wong, Ning-Cheng Lee, Ricky Lee, 2002-08-23 An engineer's guidebook demonstrating non toxic electronics manufacturing processes **IEEE 2000 First International Symposium on Quality Electronic Design** ,2000

The book delves into Integrated Circuit Defect Sensitivity Theory And Computational Models. Integrated Circuit Defect Sensitivity Theory And Computational Models is a vital topic that needs to be grasped by everyone, from students and scholars to the general public. This book will furnish comprehensive and in-depth insights into Integrated Circuit Defect Sensitivity Theory And Computational Models, encompassing both the fundamentals and more intricate discussions.

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    - Chapter 4: Integrated Circuit Defect Sensitivity Theory And Computational Models in Specific Contexts
    - Chapter 5: Conclusion
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  5. In chapter 4, this book will scrutinize the relevance of Integrated Circuit Defect Sensitivity Theory And Computational Models in specific contexts. The fourth chapter will explore how Integrated Circuit Defect Sensitivity Theory And Computational Models is applied in specialized fields, such as education, business, and technology.
  6. In chapter 5, the author will draw a conclusion about Integrated Circuit Defect Sensitivity Theory And Computational Models. This chapter will summarize the key points that have been discussed throughout the book.
- This book is crafted in an easy-to-understand language and is complemented by engaging illustrations. It is highly recommended for anyone seeking to gain a comprehensive understanding of Integrated Circuit Defect Sensitivity Theory And Computational Models.

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