

Equivalence Checking of Digital Circuits

Fundamentals, Principles, Methods

by
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Equivalence Checking of Digital Circuits Paul Molitor, Janett Mohnke, 2007-05-08 Hardware verification is the process of checking whether a design conforms to its specifications of functionality and timing. In today's design processes, it becomes more and more important. Very large scale integrated VLSI circuits and the resulting digital systems have conquered a place in almost all areas of our life, even in security sensitive applications. Complex digital systems control airplanes, have been used in banks, and on intensive care units. Hence the demand for error-free designs is more important than ever. In addition, economic reasons underline this demand as well. The design and production process of present-day VLSI circuits is highly time- and cost-intensive. Moreover, it is nearly impossible to repair integrated circuits. Thus, it is desirable to detect design errors early in the design process and not just after producing the prototype chip. All these facts are reflected by developing and production statistics of present-day companies. For example, Inneon Technologies assumed that about 60% to 80% of the overall design time was spent for verification in 2000. Other sources cite the 3 to 1 headcount ratio between verification engineers and logic designers. This shows that verifying logical correctness of the design of hardware systems is a major gate to the problem of time to market. With the chip complexity constantly increasing, the difficulty as well as the importance of functional verification of new product designs has been increased. It is not only more important to get error-free designs.

Computer Aided Verification Ruzica Piskac, Zvonimir Rakamarić, 2025-07-22 This open access 4-volume set constitutes the proceedings of the 37th International Conference on Computer Aided Verification CAV 2025 held in Zagreb, Croatia, in July 23-25, 2025. The 51 regular papers presented together with 24 tool papers, 4 case study papers in these proceedings were carefully reviewed and selected from 305 submissions. The accepted papers cover a wide spectrum of topics from theoretical results to applications of formal methods. These papers apply or extend formal methods to a wide range of domains such as concurrency, machine learning, and neural networks, quantum systems, as well as hybrid and stochastic systems. **Model**

Checking Quantum Systems Mingsheng Ying, Yuan Feng, 2021-02-04 The first book introducing computer-aided verification techniques for quantum systems with quantum computing and communication hardware. **Versatile Hardware Analysis**

Techniques Lucas Klemmer, Daniel Große, 2025-03-06 This book describes several versatile hardware analysis techniques that tackle existing and new challenges. These techniques cover different phases of the hardware development process, including verification, debugging, and post-synthesis optimization phases. The authors introduce the Waveform Analysis Language (WAL), which allows users to code analysis tasks in the form of programs that run on waveforms. The book covers processor verification, formal microcode verification, programmable automated waveform analysis demonstrated for a large variety of previously manual analysis tasks, as well as netlist optimization leveraging formal methods. All methods are available as open source, typically include examples on RISC-V analysis problems, providing a strong foundation for the community. *Parallel Computational Technologies* Leonid Sokolinsky, Mikhail Zymbler, 2023-07-24 This book constitutes the

refereed post proceedings of the 17th International Conference on Parallel Computational Technologies PCT 2023 held in Saint Petersburg Russia during March 28 30 2023 The 25 full papers included in this book were carefully reviewed and selected from 71 submissions They were organized in topical sections as follows High Performance Architectures Tools and Technologies Parallel Numerical Algorithms and Supercomputer Simulation **Machine Learning Applications in Electronic Design Automation** Haoxing Ren,Jiang Hu,2023-01-01 This book serves as a single source reference to key machine learning ML applications and methods in digital and analog design and verification Experts from academia and industry cover a wide range of the latest research on ML applications in electronic design automation EDA including analysis and optimization of digital design analysis and optimization of analog design as well as functional verification FPGA and system level designs design for manufacturing DFM and design space exploration The authors also cover key ML methods such as classical ML deep learning models such as convolutional neural networks CNNs graph neural networks GNNs generative adversarial networks GANs and optimization methods such as reinforcement learning RL and Bayesian optimization BO All of these topics are valuable to chip designers and EDA developers and researchers working in digital and analog designs and verification **Design Automation for Field-coupled Nanotechnologies** Marcel Walter,Robert Wille, Frank Sill Torres,Rolf Drechsler,2022-01-10 This book discusses the main tasks of Design Automation for Field coupled Nanocomputing FCN technologies in order to enable large scale composition of elementary building blocks that obtain correct systems from given function specifications To this end a holistic design flow is described which covers exact and scalable placement routing one pass logic synthesis novel clocking mechanisms for data synchronization and formal verification for obtained circuit layouts Additionally theoretical groundwork is presented that lays the foundation for any algorithmic consideration in the future Furthermore an open source FCN design framework called fiction which contains implementations of all proposed techniques is presented and made publicly available The approaches discussed in this book address obstacles that have existed since the conceptualization of the FCN paradigm and could not be resolved since then As a result this book substantially advances the state of the art in design automation for FCN technologies **Kompaktkurs VHDL** Paul Molitor,Jörg Ritter,2013-01-28 Das Buch umfasst den Stoff einer einsemestrigen Vorlesung und bietet dem Leser eine leicht verständliche und mit vielen interessanten Beispielen unterlegte Einführung in die Sprache Die Autoren verzichten bewusst auf die Erläuterung nur selten benutzter Konstrukte und konzentrieren ihre Darstellung auf die Betrachtung der Sprache unter dem Aspekt der Schaltkreissynthese Das Buch verbindet Theorie und praktische Anwendungsbeispiele

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